SP-2772: Mid.CBF Hardware Refresh Agilex investigation III

CIP-1148, CIP-1149, CIP-1150: 400GE Tester

Stephen Harrison
National Research Council Canada

Goals

The previous demo (SP-2093) showed:

- basic interoperability between the Edge-Core DCS810 400GE switch and the Intel I-Series FPGA F-Tile 400GE subsystem.
- generic packet traffic up to 320 Gbps (80%) using Intel example design, multicast to all ports, and looped back to the same switch.

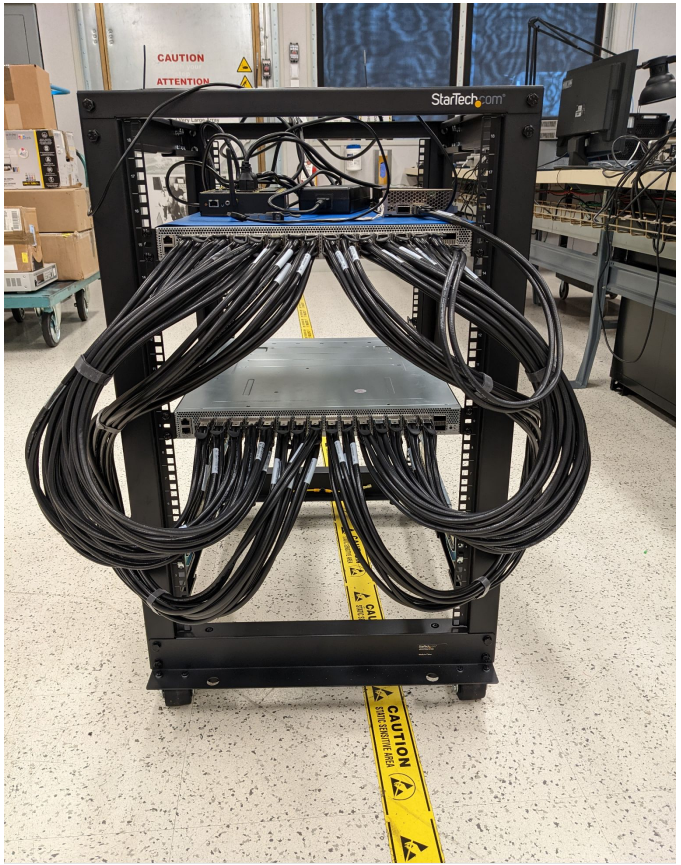
This demo (SP-2772) builds upon the previous demo to show:

- a 400GE tester FPGA design based on an array of SPFRx packetizers, up to 54 independent streams, able to achieve 100% link utilization.
- modification of Ethernet standard and custom header fields (from SPFRx to CSP ICD) within the tester switch, to emulate multiple frequency slice streams.
- forwarding of packets based on parsing custom header fields in the DUT switch.

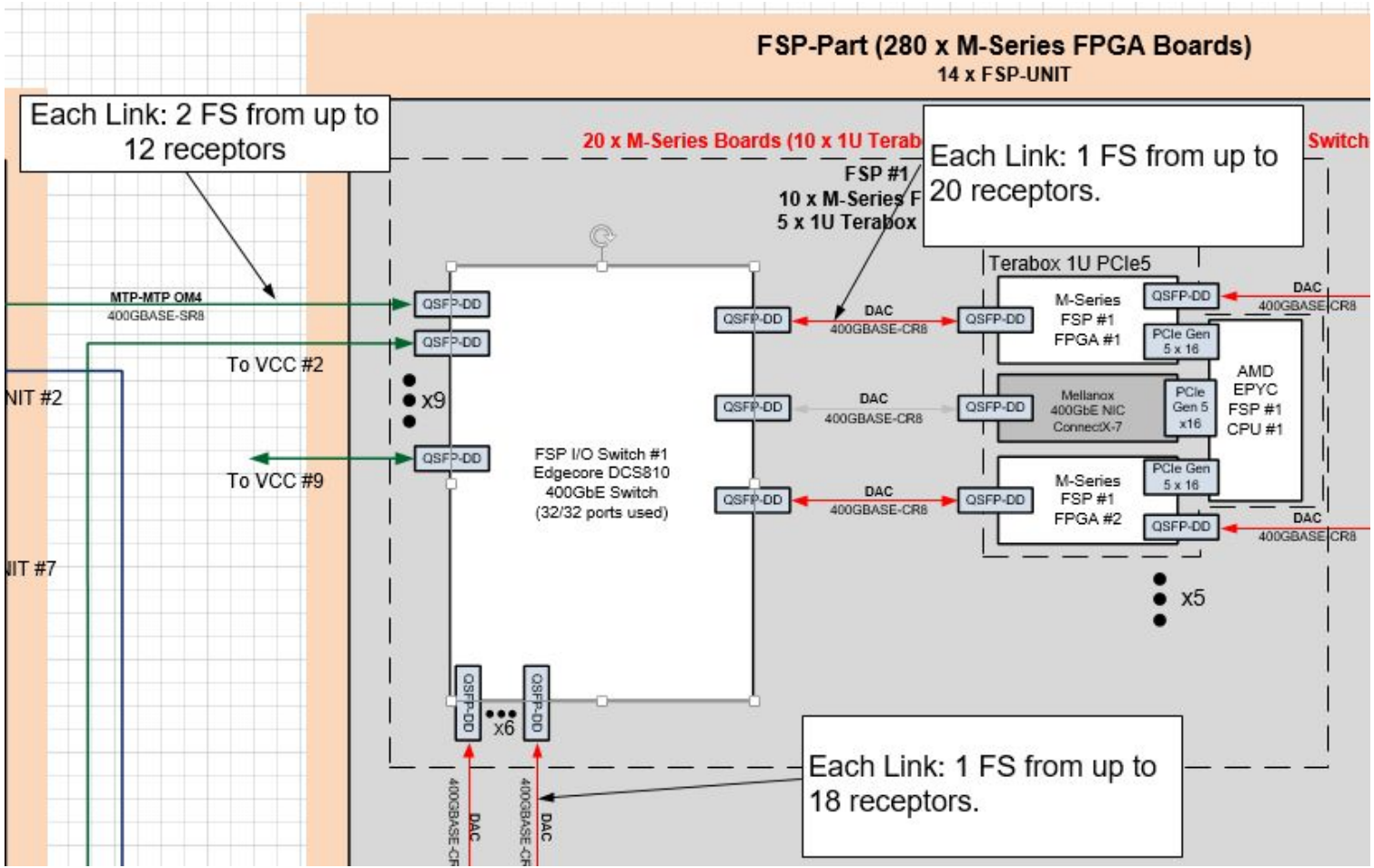
Hardware Setup

- Intel I-Series Development Kit connected to test switch, port 32 via 400G DAC cable

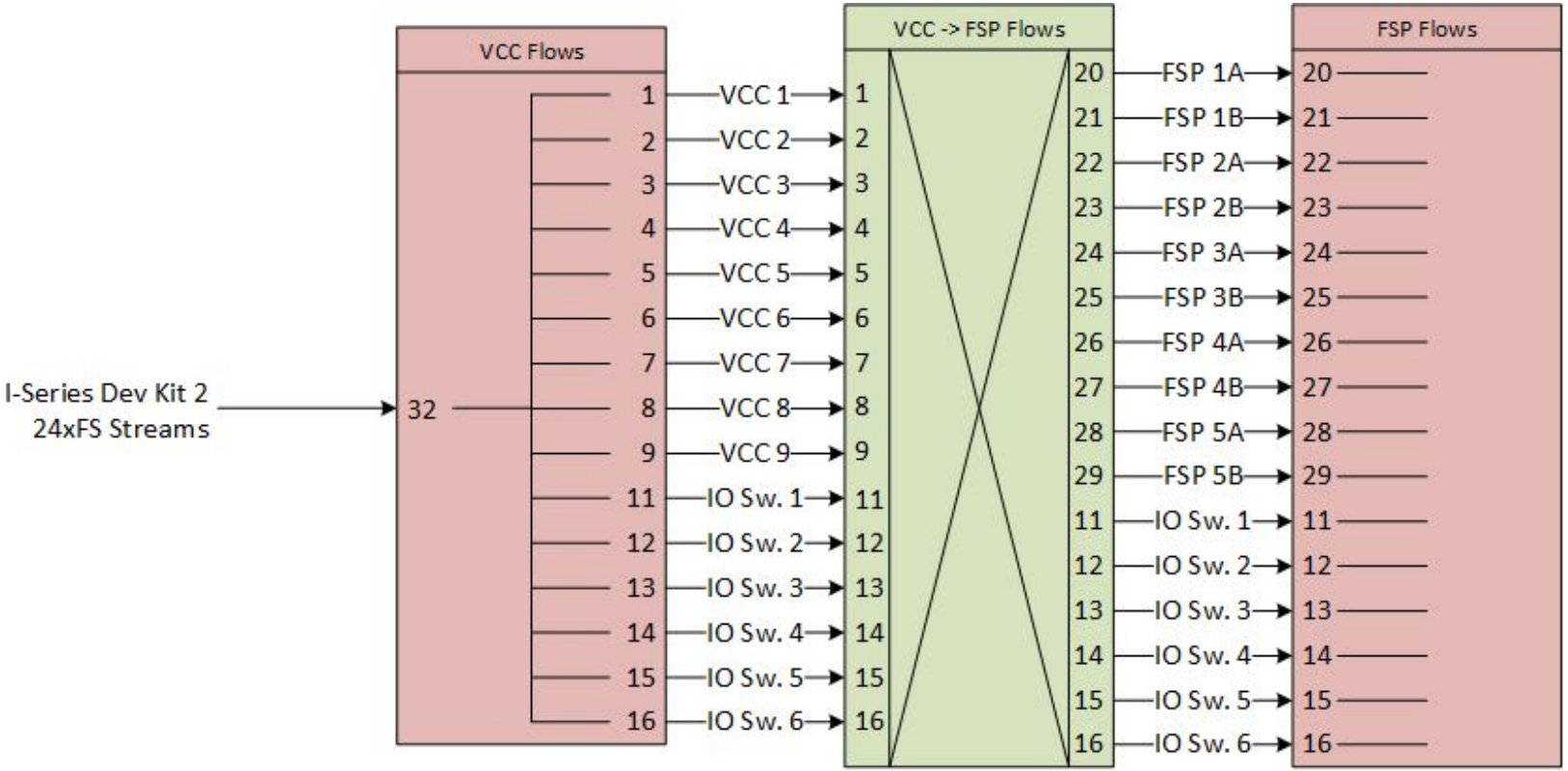
- Ports 1-29 on test switch and DUT switch connected via 400G DAC cables



System Context



Datapath Setup



Datapath Setup

- 24 generic streams at the “Frequency Slice” rate enter the tester switch.
  - Streams are multicast to 9 “VCC” and 6 “I/O switch” output ports.
  - Multicast streams are updated with unique MAC Address, DISH ID and FS ID values.
  - 9 “VCC” output ports emulate 2 FS from up to 12 antennas (DISH 0-107, FS 5-6, for demonstration).
  - 6 “I/O Switch” output ports emulate 1 FS from up to 18 antennas (DISH 108-215, FS 5, for demonstration).

- The DUT switch receives 9 “VCC” Streams and 6 “I/O Switch” streams.
  - The DUT switch routes packets to physical ports based on {DISH ID, FS ID}
  - Frequency slice 5, in groups of 20 antennas, is sent to the 10 FSP outputs.
  - Frequency slice 6, in groups of 18 antennas, is sent to the 6 I/O Switch outputs.

- The test switch receives the streams and shows the received rate.
  - Packets are counted on a Dish ID, FS ID basis to check that we send and receive the same number of packets.

Packet Parsing

	Byte 0		Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
Word/Bit	**B0**	**B7**	**B8**	**B16**	**B24**	**B32**	**B40**	**B48**	**B56**	**B63**
W0	Source MAC address							Destination MAC----		
W1	----address					0x4653 (“FS”)		Dish ID	FS ID	
W2	Band_ID (R.2.2)		Unassigned							
W3	Packet counter from 1PPS (R.23)					No. of time samples in packet (R.2.4)		Unassigned	No. of Frames (R.2.7)	
W4	Transport sample rate (R.71)							Noise diode states (R.2.6)	Noise diode change Frame (R.2.6)	
W5	UTC time code (R.2.3)					Noise Diode transition holdoff count		Unassigned		
W6	No. of time samples from 1PPS (R.2.5)							Unassigned		
W7	Hardware Source ID (R.43)									

Figure 2-2 Meta_Frame format.

Demo

1. Start P4 programs in switch daemon.
2. Configure DUT switch runtime:
    a. Set up ports: 400G-R8, RS-FEC, disable auto-negotiation on port 32.
    b. Set up packet replication engine (multicast group).
    c. Configure header modification tables (update DISH and FS ID).
3. Configure Tester switch runtime:
    a. Set up ports.
    b. Set up FS/DISH routing table.
4. Set up 400GE Tester FPGA.
    a. Set up 24 generic streams.
    b. Run traffic, show data rates.
    c. Stop traffic, show packet counts.