Speed-up study - Agilex FPGA

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for the PSS Team

Feature: SP-1782

25 Aug 2021

Objective: Research new FPGA development environments

- OneAPI Development Environments
- Executing VHDL from OpenCL/OneAPI on a Single Host
- **Benchmark Performance Tests of Agilex FPGA Using VHDL**

OpenCL and OneAPI Environments have dependency on Intel

Motivation

Prototype development so far has used what are now legacy FPGAs and associated development environments. The PSS Production solution will use latest FPGAs and development environments. This Feature aims to understand the impact of using up-to-date FPGA development environments to help reduce future FPGA development / code porting risk

OneAPI is based on a SYCL

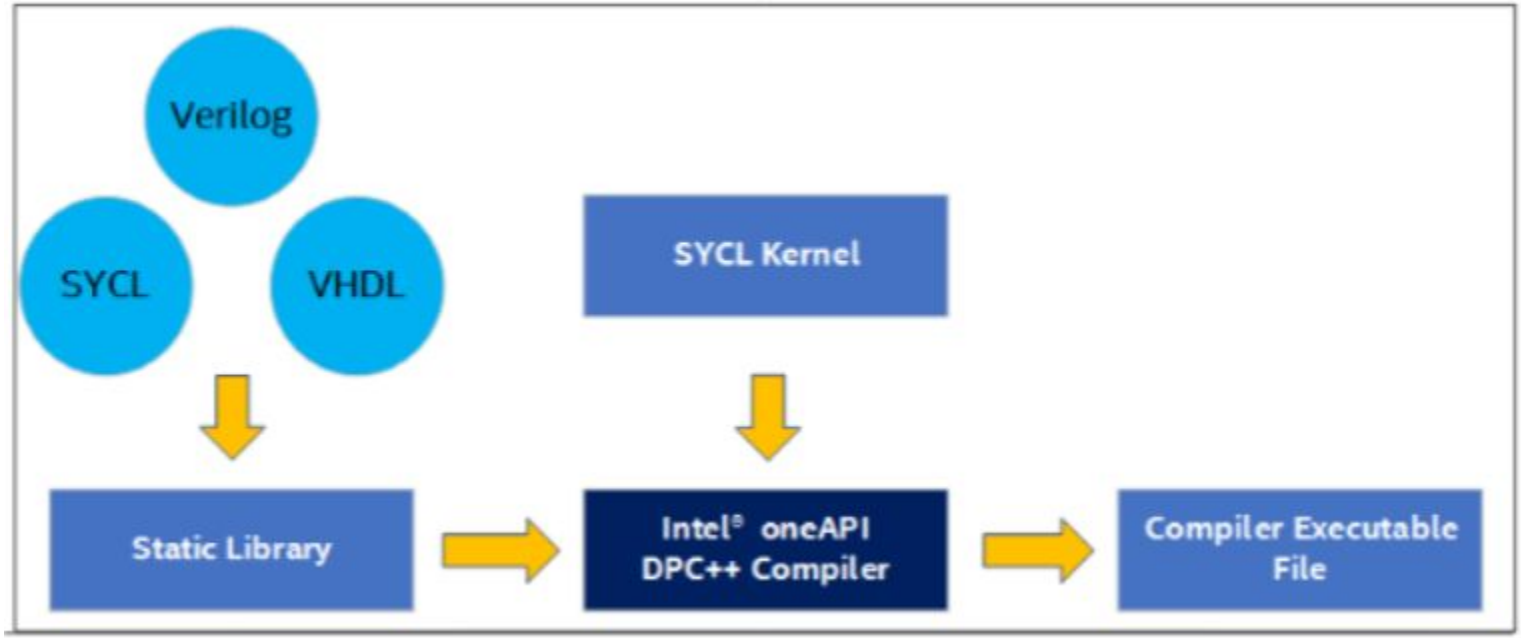
- Same C++ code for CPU, GPU and FPGA
- Open Source
- We have installed OneAPI environment and tried basic example codes

```
dsp@RRI-D-544:~/DISK2/ONEAPIFPGA/vector-add$ ./vector-add-buffers.fpga_emu
Running on device: Intel(R) FPGA Emulation Device
Vector size: 10000
[0]: 0 + 0 = 0
[1]: 1 + 1 = 2
[2]: 2 + 2 = 4
...
[9999]: 9999 + 9999 = 19998
Vector add successfully completed on device.
dsp@RRI-D-544:~/DISK2/ONEAPIFPGA/vector-add$ ./vector-add-buffers
Running on device: AMD Ryzen 9 3900X 12-Core Processor
Vector size: 10000
[0]: 0 + 0 = 0
[1]: 1 + 1 = 2
[2]: 2 + 2 = 4
...
[9999]: 9999 + 9999 = 19998
Vector add successfully completed on device.
dsp@RRI-D-544:~/DISK2/ONEAPIFPGA/vector-add$
```

AT4-507 Comparison of Compilation, Execution, Debugging flows between oneAPI and OpenCL

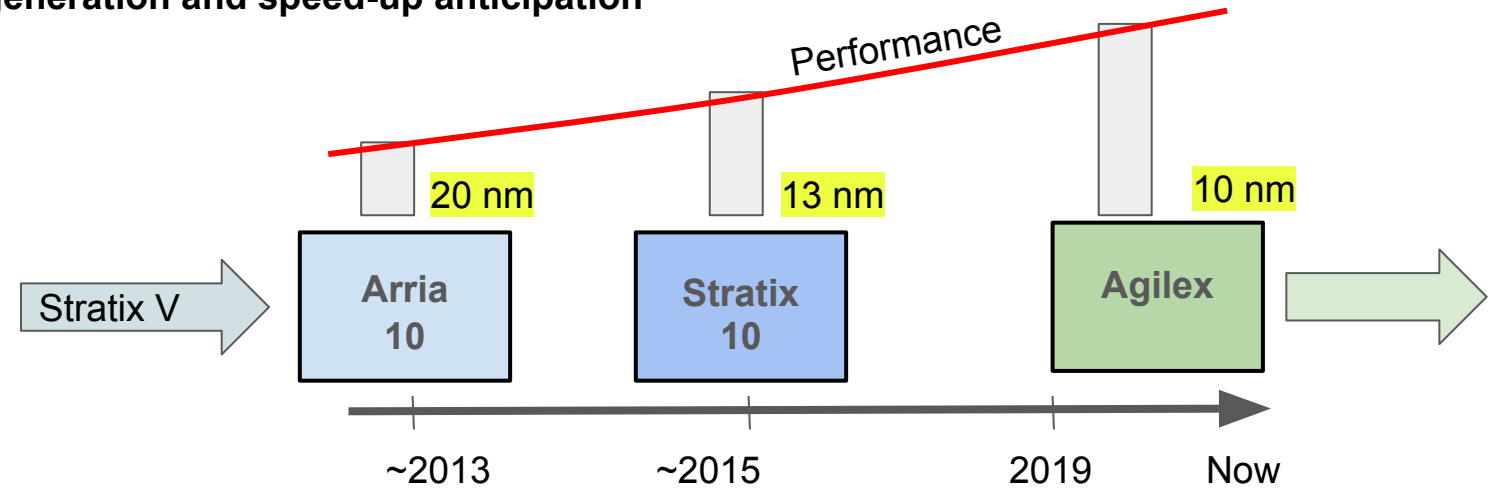
Executing VHDL libraries from OpenCL/OneAPI

- VHDL codes included as a Static library (ongoing work)



Performance Tests

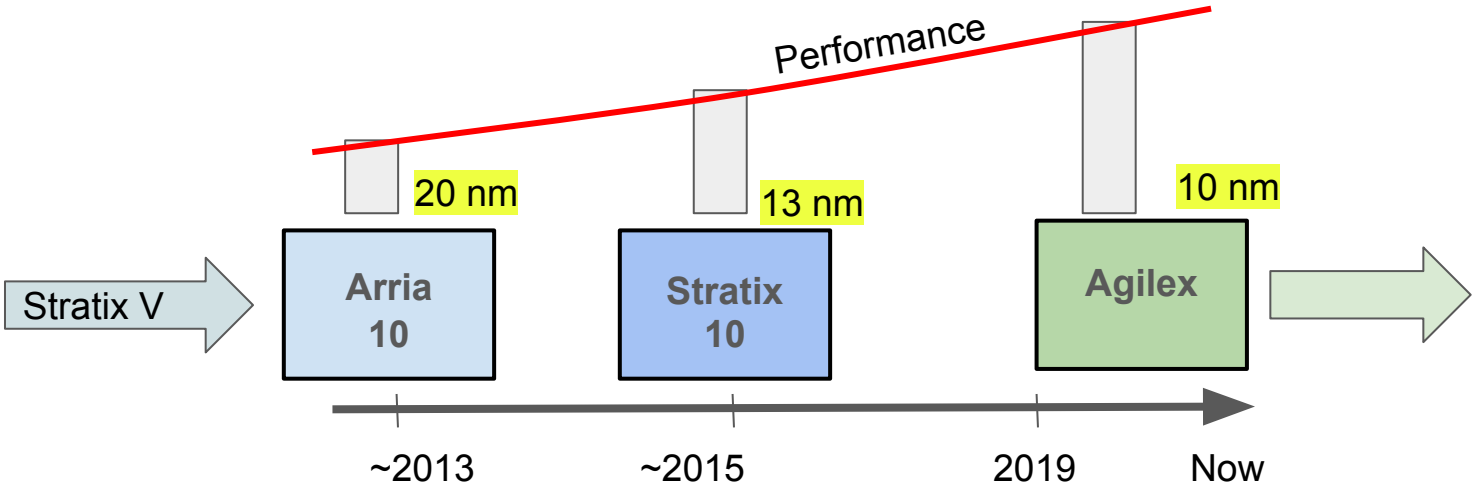
FPGA generation and speed-up anticipation



Performance Tests of Agilex FPGA Using VHDL

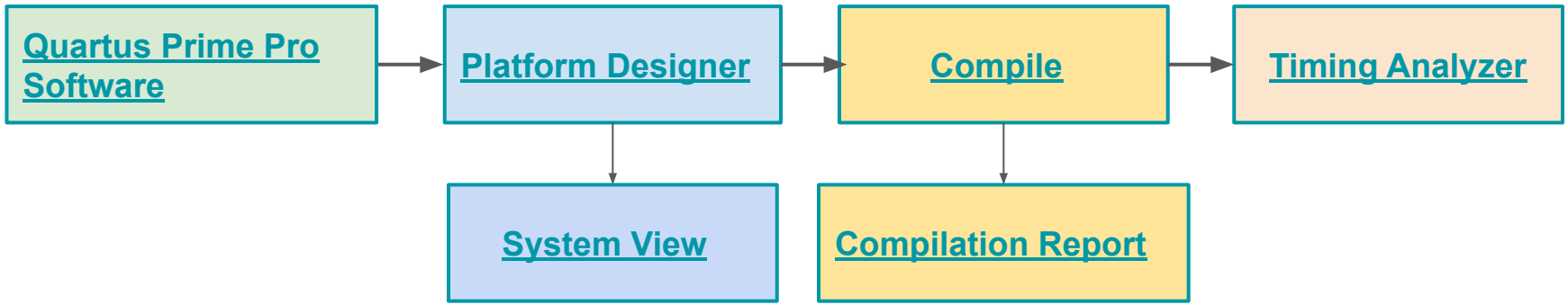
Signal processing VHDL library codes (eg., **FFT**, FIR etc) configured with varying complexity (data length etc) and compiled for a **mid-speed grade, mid-size Agilex FPGA** using the intel **Quartus** 21.1 software.

The **speed performance** compared with three generations of FPGAs

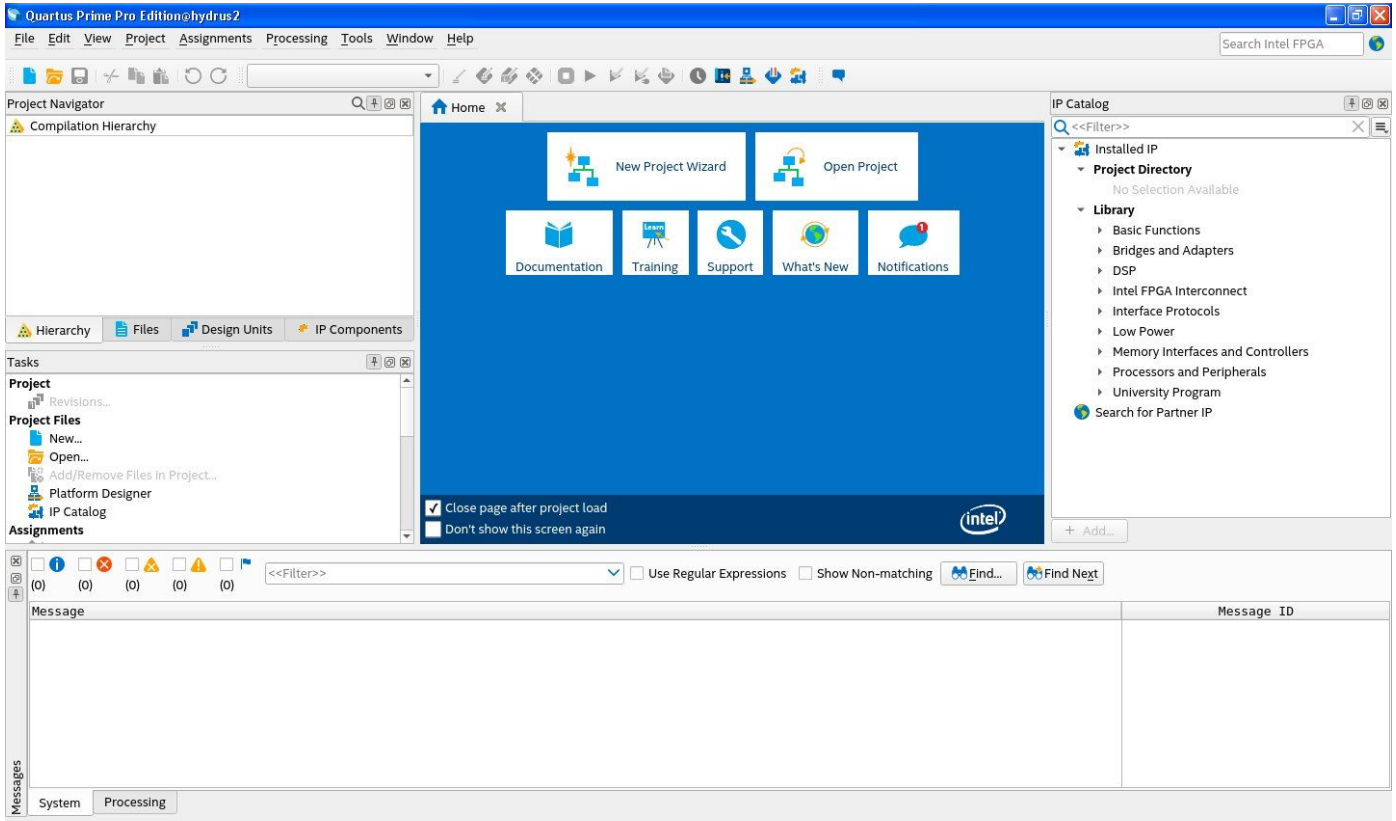


Performance Tests of Agilex FPGA Using VHDL

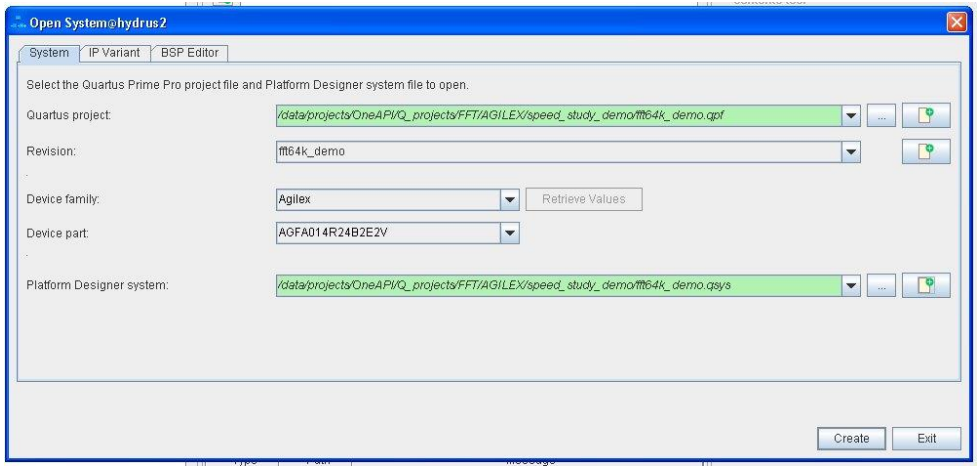
Quartus design flow

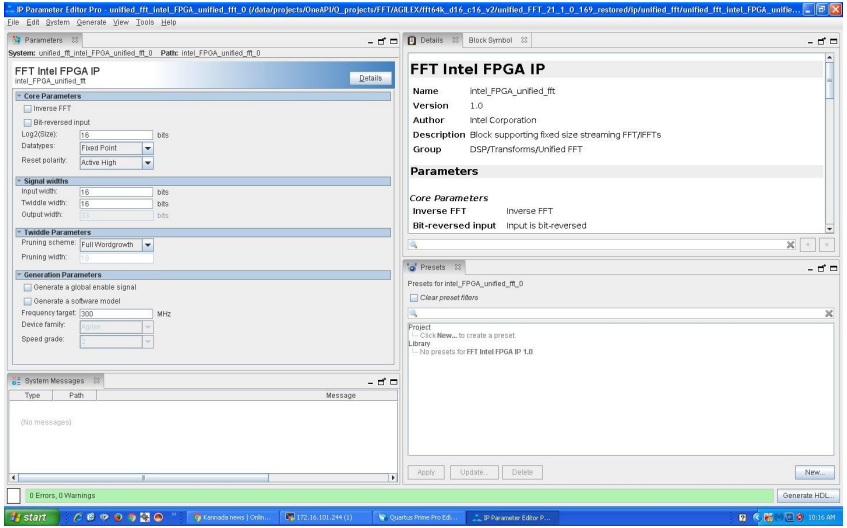


Quartus Prime Pro Edition Software

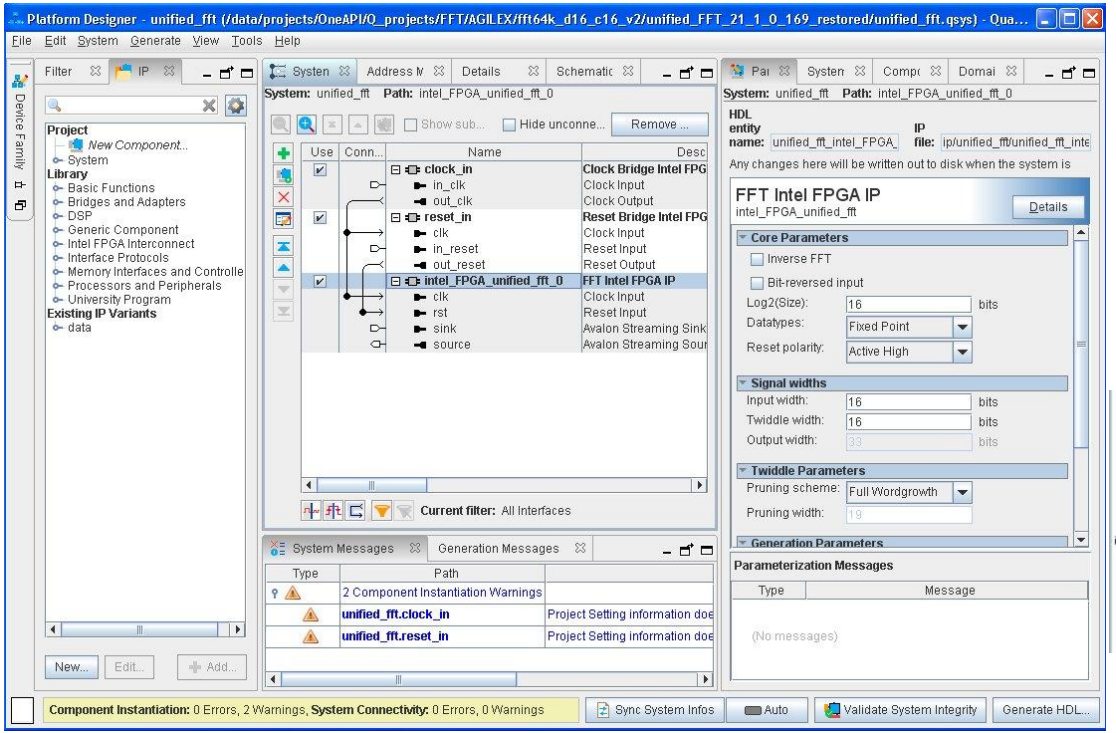


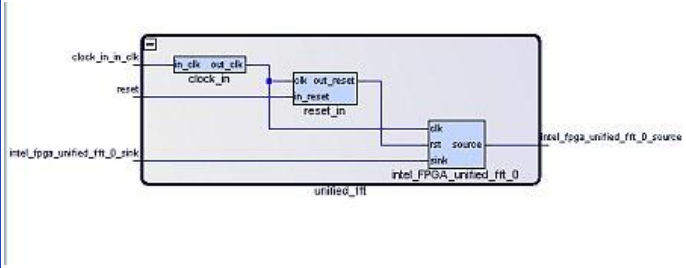
Creating Quartus project



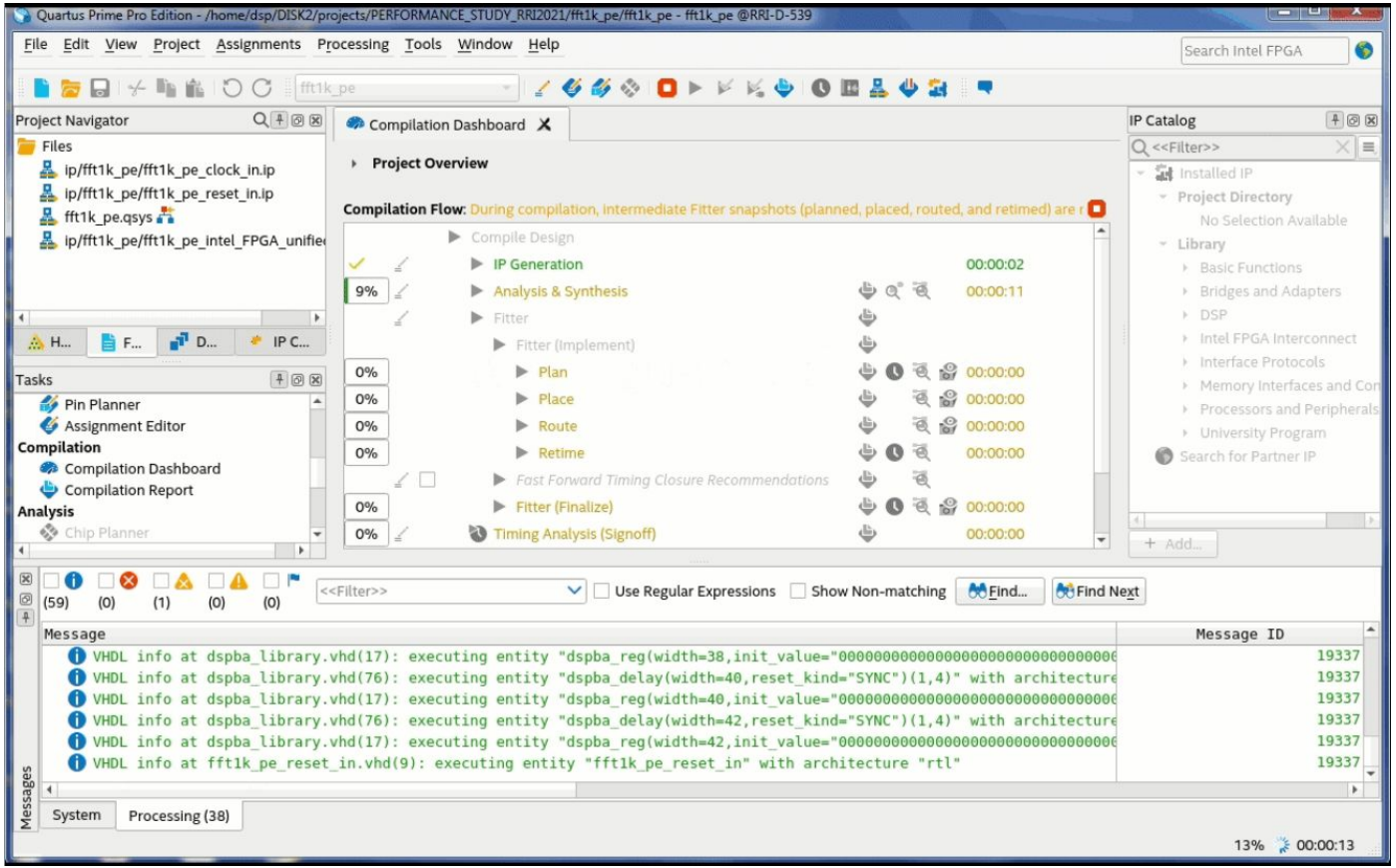


Platform Designer- System view

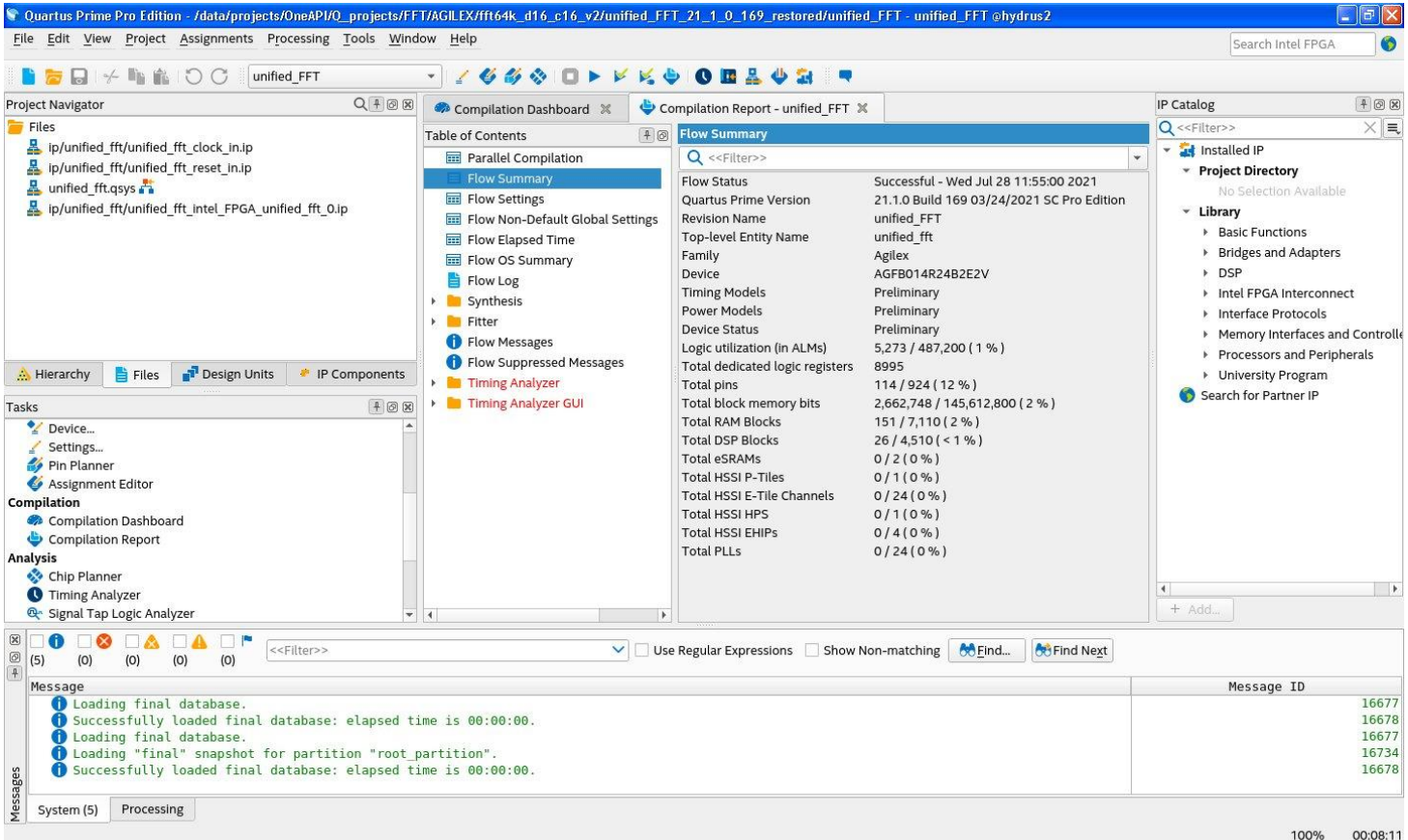




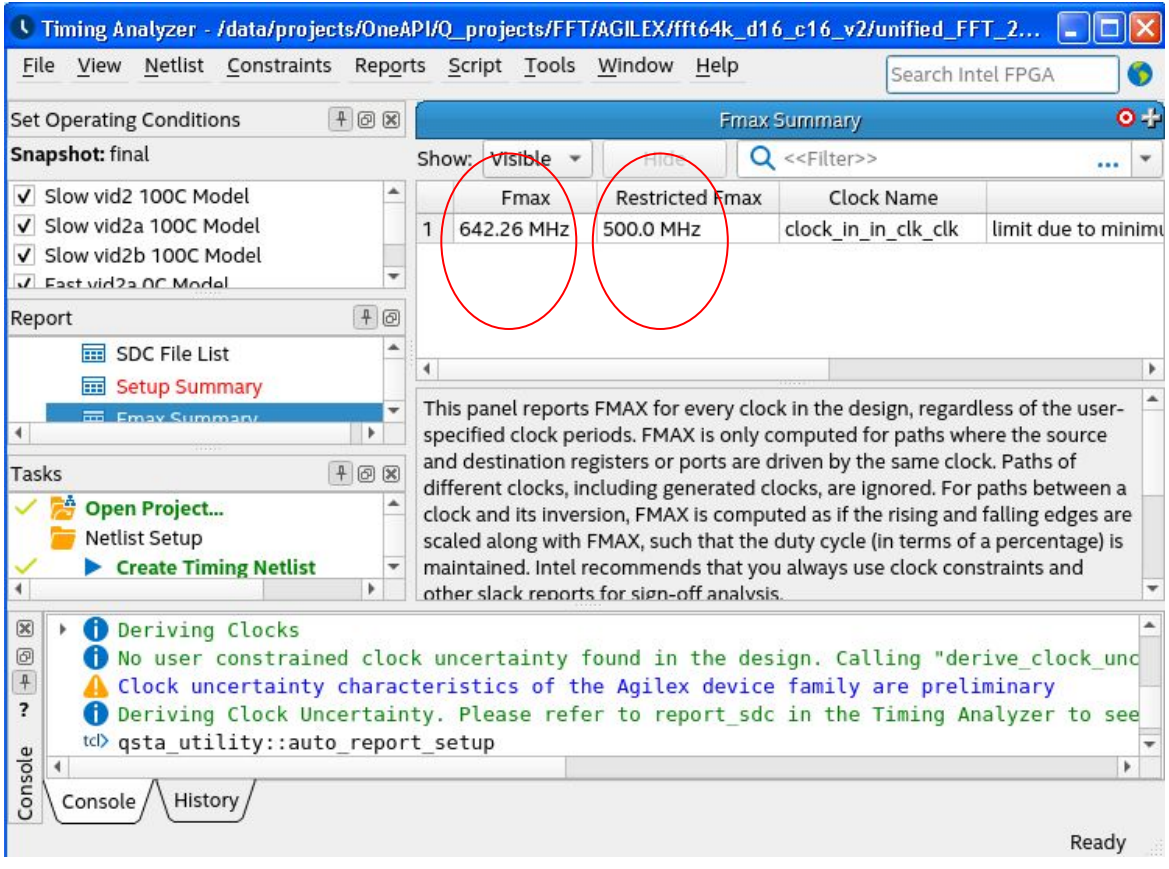
Project Compilation flow



Compiled Resource Summary

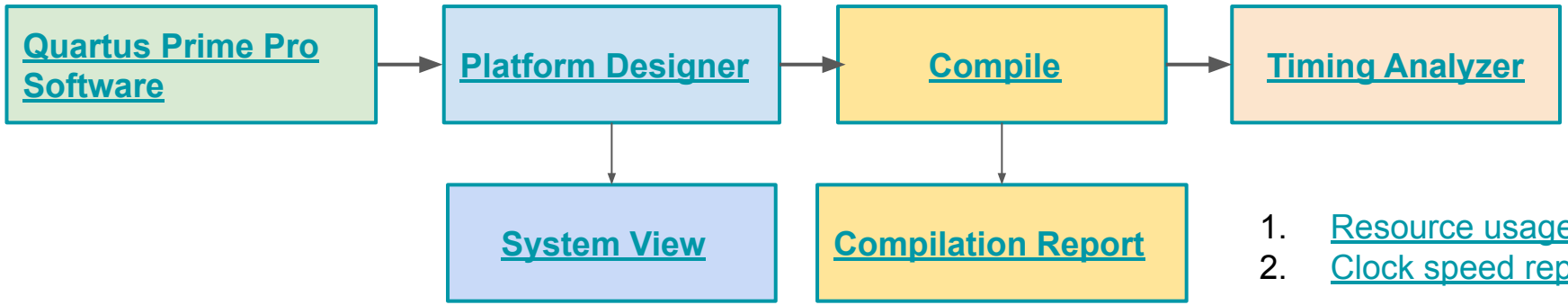


Timing Analyzer report



Performance Tests of Agilex FPGA Using VHDL

Quartus design flow



1. Resource usage
2. Clock speed report

FFT IP
1 k to 64 k point

Results

QUARTUS :	21.1		IP Used :	FFT Intel FPGA IP				
DEVICE :	Agilex: AGFB014R24B2E2V		Core Speed : 2					
Sl. No	Design Name	FFT Length	ALM (487,200)	Block Mem(145,612,800)	RAM (7,110)	DSP (4,510)	Restricted Fmax (MHz)	Fmax (MHz)
1	fft1k_d16_c16	1024	2,365	35,480	7	14	500	657.89
2	fft2k_d16_c16	2048	2,519	80,226	11	18	500	657.46
3	fft4k_d16_c16	4096	2,841	161,804	15	18	500	657.46
4	fft8k_d16_c16	8192	3,317	331,480	24	22	500	657.89
5	fft16k_d16_c16	16384	3,654	666,756	46	22	500	652.32
6	fft32k_d16_c16	32768	4,504	1,345,716	81	26	500	657.89
7	fft64k_d16_c16	65536	5,273	2,662,748	151	26	500	642.26

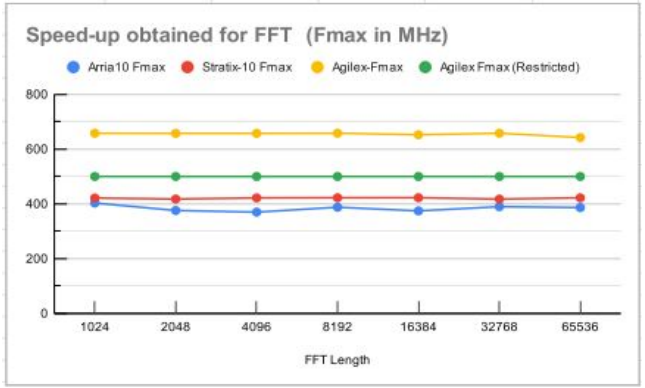
Agilex

DEVICE :	Stratix 10: 1SG280LN2F43E2VG		Core Speed : 2					
Sl. No	Design Name	FFT Length	ALM (933,120)	Block Mem(240,046,080)	RAM (11,721)	DSP (5,760)	Restricted Fmax (MHz)	Fmax (MHz)
1	fft1k_d16_c16	1024	1,712	35,328	7	14	421.41	421.41
2	fft2k_d16_c16	2048	1,910	79,956	11	18	417.54	417.54
3	fft4k_d16_c16	4096	2,125	161,564	15	18	421.76	421.76
4	fft8k_d16_c16	8192	2,488	331,160	24	22	422.3	422.3
5	fft16k_d16_c16	16384	2,723	666,428	45	22	422.48	422.48
6	fft32k_d16_c16	32768	3,218	1,345,270	79	26	417.36	417.36
7	fft64k_d16_c16	65536	3,725	2,662,246	150	26	422.12	422.12

Stratix-10

DEVICE :	Arria 10: 10AX115H3F34I2SG		Core Speed : 2					
Sl. No	Design Name	FFT Length	ALM (427,200)	Block Mem(55,562,240)	RAM (2,713)	DSP (1,518)	Restricted Fmax (MHz)	Fmax (MHz)
1	fft1k_d16_c16	1024	1,450	38,224	9	14	403.06	403.06
2	fft2k_d16_c16	2048	1,664	80,500	11	18	375.94	375.94
3	fft4k_d16_c16	4096	1,848	162,204	15	18	369.82	369.82
4	fft8k_d16_c16	8192	2,118	331,960	24	22	387.75	387.75
5	fft16k_d16_c16	16384	2,316	667,608	46	22	374.39	374.39
6	fft32k_d16_c16	32768	2,678	1,347,172	81	26	389.71	389.71
7	fft64k_d16_c16	65536	2,885	2,665,640	149	26	386.55	386.55

Arria-10



Results

QUARTUS :	21.1	
DEVICE :	Agilex: AGFB014R24B2E2V	
Sl. No	Design Name	FFT Le
1	fft1k_d16_c16	102
2	fft2k_d16_c16	204
3	fft4k_d16_c16	409
4	fft8k_d16_c16	819
5	fft16k_d16_c16	1638
6	fft32k_d16_c16	3276
7	fft64k_d16_c16	6553

Agilex

DEVICE :	Stratix 10: 1SG280LN2F43E2VG	
Sl. No	Design Name	FFT Le
1	fft1k_d16_c16	102
2	fft2k_d16_c16	204
3	fft4k_d16_c16	409
4	fft8k_d16_c16	819
5	fft16k_d16_c16	1638
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Stratix-10

DEVICE :	Arria 10: 10AX115H3F34I2SG	
Sl. No	Design Name	FFT Le
1	fft1k_d16_c16	102
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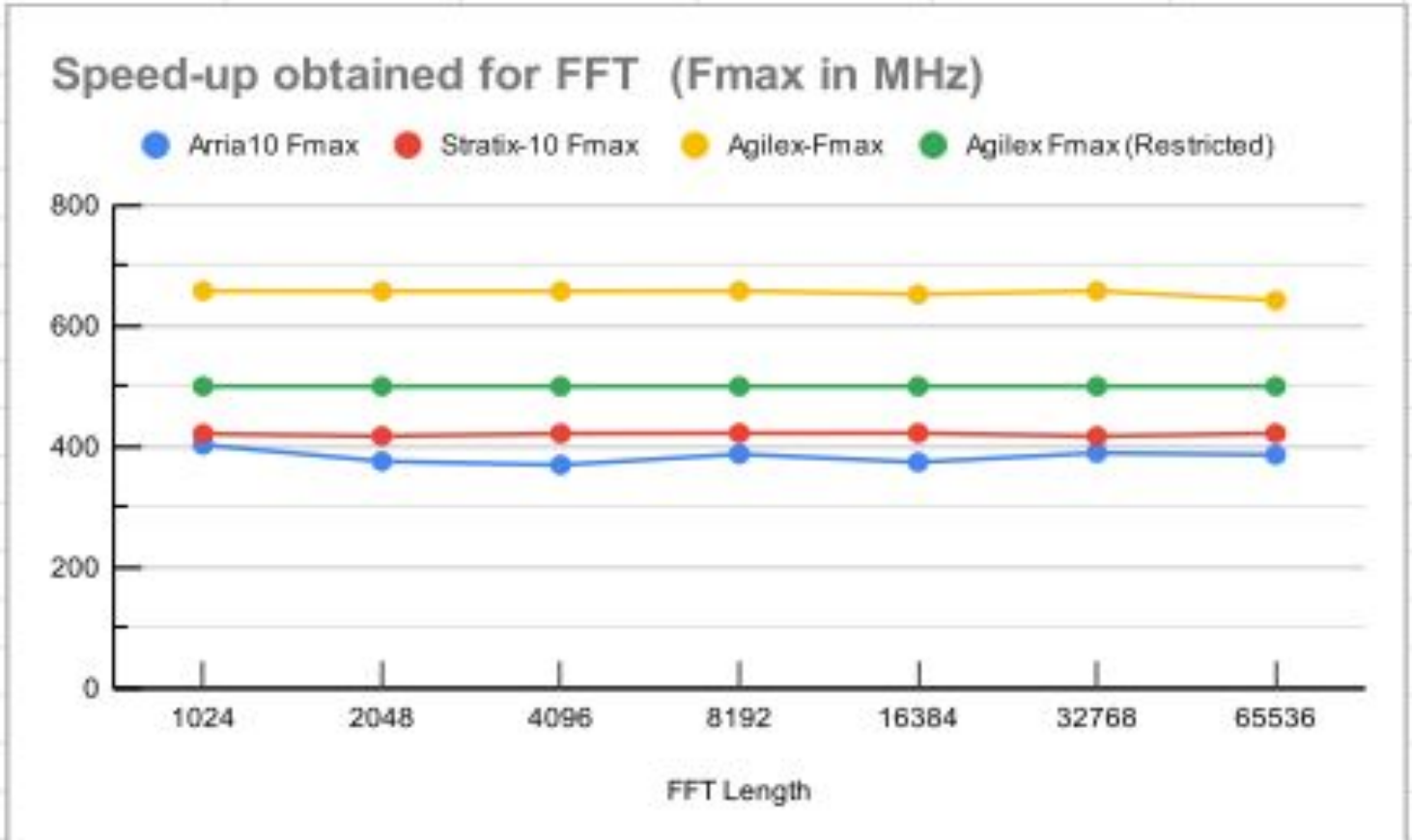
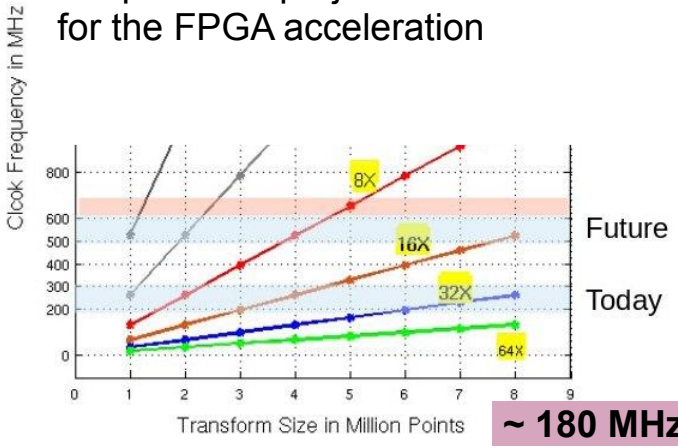
Arria-10



Results match with
our pre 2017 projection
for the FPGA acceleration



~ 180 MHz .

~380 MHz

~ 200 MHz .

~420 MHz

~ 250 - 300 MHz .

~ 500 - 600 MHz .

Performance

20 nm

13 nm

10 nm

Stratix V

Arria 10

Stratix 10

Agilex

~2013

~2015

2019

Now

THANK YOU