

# Speed-up study - Agilex FPGA

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for the PSS Team

Feature: SP-1782

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## **Objective:** Research new FPGA development environments

- OneAPI Development Environments
- Executing VHDL from OpenCL/OneAPI on a Single Host
- **Benchmark Performance Tests of Agilex FPGA Using VHDL**

OpenCL and OneAPI Environments have dependency on Intel

## **Motivation**

Prototype development so far has used what are now legacy FPGAs and associated development environments. The PSS Production solution will use latest FPGAs and development environments. This Feature aims to understand the impact of using up-to-date FPGA development environments to help reduce future FPGA development / code porting risk

# OneAPI is based on a [SYCL](#)

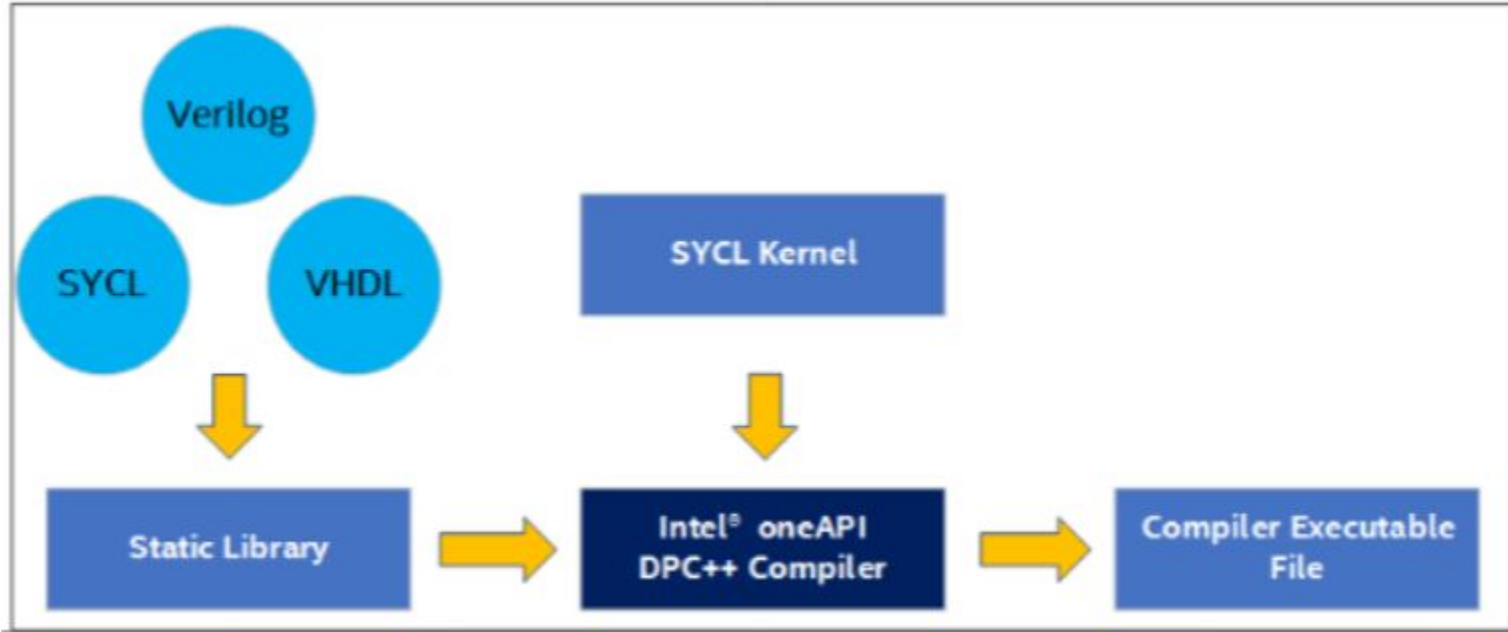
- Same C++ code for CPU, GPU and FPGA
- Open Source
- We have installed OneAPI environment and tried basic example codes

```
dsp@RRI-D-544:~/DISK2/ONEAPI/FPGA/vector-add$ ./vector-add-buffers.fpga_emu
Running on device: Intel(R) FPGA Emulation Device
Vector size: 10000
[0]: 0 + 0 = 0
[1]: 1 + 1 = 2
[2]: 2 + 2 = 4
...
[9999]: 9999 + 9999 = 19998
Vector add successfully completed on device.
dsp@RRI-D-544:~/DISK2/ONEAPI/FPGA/vector-add$ ./vector-add-buffers
Running on device: AMD Ryzen 9 3900X 12-Core Processor
Vector size: 10000
[0]: 0 + 0 = 0
[1]: 1 + 1 = 2
[2]: 2 + 2 = 4
...
[9999]: 9999 + 9999 = 19998
Vector add successfully completed on device.
dsp@RRI-D-544:~/DISK2/ONEAPI/FPGA/vector-add$
```

[AT4-507 Comparison of Compilation, Execution, Debugging flows between oneAPI and OpenCL](#)

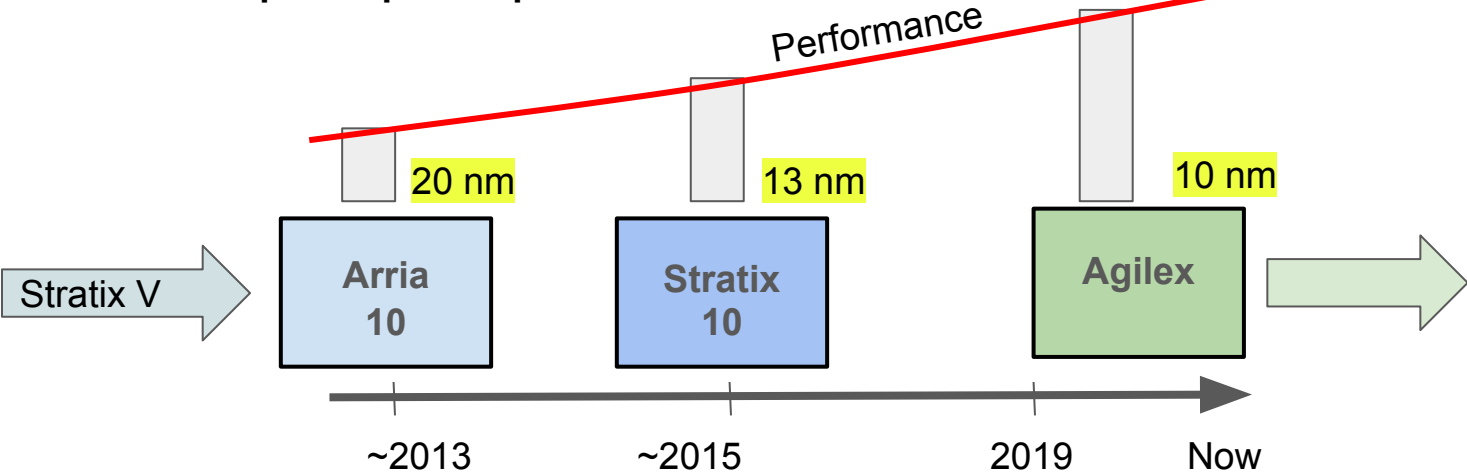
## Executing VHDL libraries from OpenCL/OneAPI

- VHDL codes included as a Static library (ongoing work)



# Performance Tests

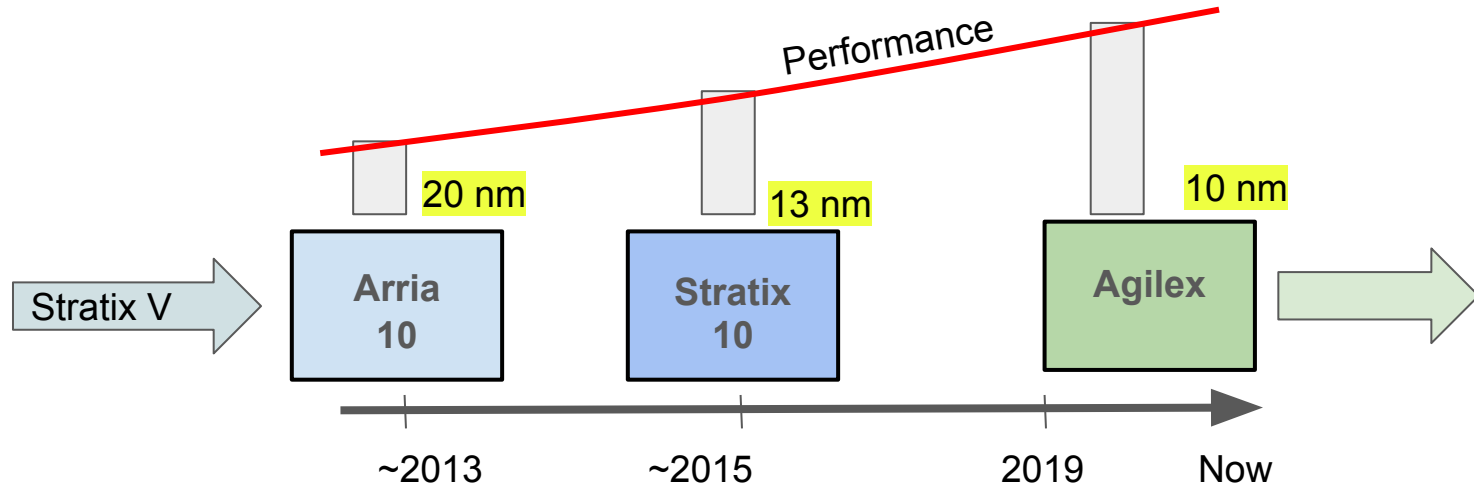
## FPGA generation and speed-up anticipation



## Performance Tests of Agilex FPGA Using VHDL

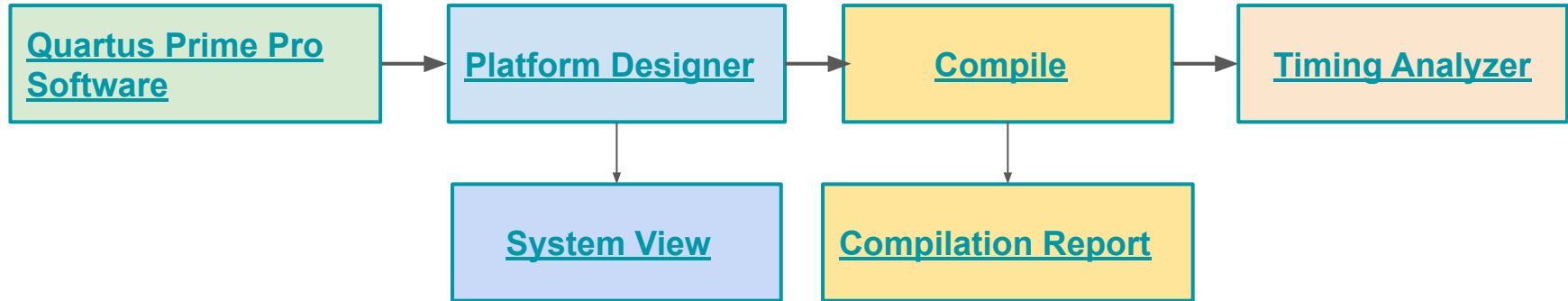
Signal processing VHDL library codes (eg., **FFT**, **FIR** etc) configured with varying complexity (data length etc) and compiled for a **mid-speed grade, mid-size Agilex FPGA** using the intel **Quartus 21.1** software.

The **speed performance** compared with three generations of FPGAs

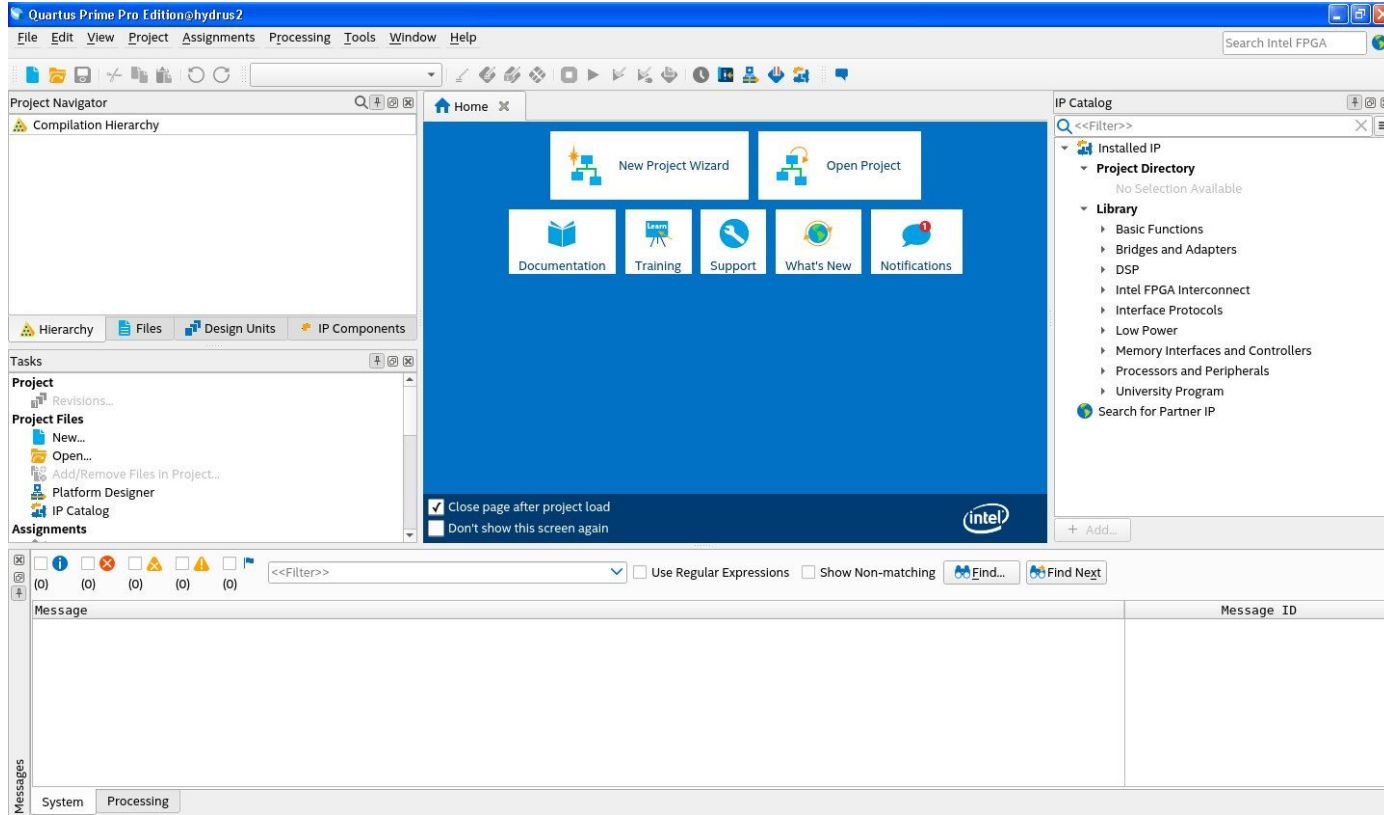


## Performance Tests of Agilex FPGA Using VHDL

### Quartus design flow

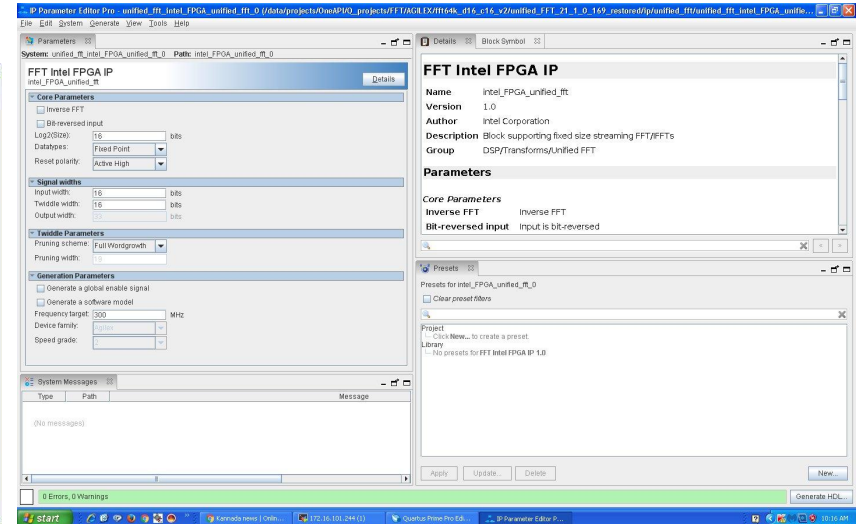
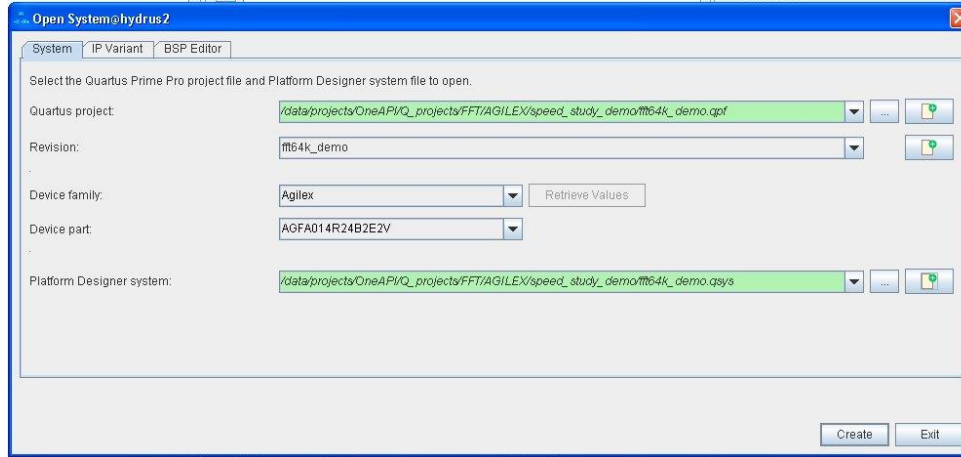


# Quartus Prime Pro Edition Software





# Creating Quartus project

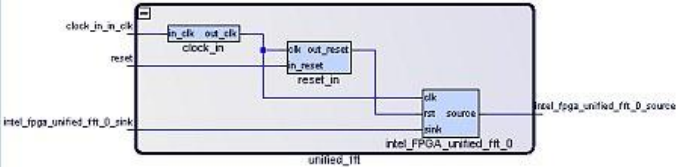


# Platform Designer- System view

The screenshot displays the Platform Designer interface for a system named 'unified\_fft'. The main window is divided into several panes:

- Project:** Shows the current project path: /data/projects/OneAPI/Q\_projects/FFT/AGILEX/fft64k\_d16\_c16\_v2/unified\_FFT\_21\_1\_0\_169\_restored/unified\_fft.qsys.
- Library:** Lists various components like Basic Functions, Bridges and Adapters, DSP, Generic Component, Intel FPGA Interconnect, Interface Protocols, Memory Interfaces and Controls, Processors and Peripherals, and University Program.
- System Messages:** A table showing warnings for component instantiation.
- System View:** A hierarchical tree of components. The 'intel\_fpga\_unified\_fft\_0' component is selected, showing its internal sub-components: clock\_in (with in\_clk and out\_clk), reset\_in (with in\_reset and out\_reset), and the FFT Intel FPGA IP (with clk, rst, sink, and source).
- Details:** A configuration panel for the selected 'FFT Intel FPGA IP' component. It includes:
  - Core Parameters:** Inverse FFT (unchecked), Bit-reversed input (unchecked), Log2(Size) set to 16, Datatypes set to Fixed Point, and Reset polarity set to Active High.
  - Signal widths:** Input width: 16 bits, Twiddle width: 16 bits, Output width: 33 bits.
  - Twiddle Parameters:** Pruning scheme: Full Wordgrowth, Pruning width: 19.
  - Generation Parameters:** A section for parameterization messages, currently showing '(No messages)'. Below this is a 'Parameterization Messages' table with columns for Type and Message.

At the bottom of the window, a status bar indicates: **Component instantiation: 0 Errors, 2 Warnings, System Connectivity: 0 Errors, 0 Warnings**. Buttons for 'Sync System Infos', 'Auto', 'Validate System Integrity', and 'Generate HDL...' are also visible.



# Project Compilation flow

Quartus Prime Pro Edition - /home/dsp/DISK2/projects/PERFORMANCE\_STUDY\_RRI2021/fft1k\_pe/fft1k\_pe - fft1k\_pe @RRI-D-539

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

Project Navigator

- Files
  - ip/fft1k\_pe/fft1k\_pe\_clock\_in.ip
  - ip/fft1k\_pe/fft1k\_pe\_reset\_in.ip
  - fft1k\_pe.qsys
  - ip/fft1k\_pe/fft1k\_pe\_Intel\_FPGA\_unfiled

Tasks

- Pin Planner
- Assignment Editor
- Compilation
  - Compilation Dashboard
  - Compilation Report
- Analysis
  - Chip Planner

Compilation Dashboard

Project Overview

Compilation Flow: During compilation, intermediate Fitter snapshots (planned, placed, routed, and retimed) are r

- Compile Design
  - IP Generation 00:00:02
  - Analysis & Synthesis 00:00:11
  - Fitter
    - Fitter (Implement)
      - Plan 00:00:00
      - Place 00:00:00
      - Route 00:00:00
      - Retime 00:00:00
    - Fast Forward Timing Closure Recommendations
    - Fitter (Finalize) 00:00:00
    - Timing Analysis (Signoff) 00:00:00

IP Catalog

Installed IP

- Project Directory
  - No Selection Available
- Library
  - Basic Functions
  - Bridges and Adapters
  - DSP
  - Intel FPGA Interconnect
  - Interface Protocols
  - Memory Interfaces and Co
  - Processors and Peripherals
  - University Program
- Search for Partner IP

Messages

Message	Message ID
VHDL info at dspba_library.vhd(17): executing entity "dspba_reg(width=38,init_value="00000000000000000000000000000000"	19337
VHDL info at dspba_library.vhd(76): executing entity "dspba_delay(width=40,reset_kind="SYNC")(1,4)" with architecture	19337
VHDL info at dspba_library.vhd(17): executing entity "dspba_reg(width=40,init_value="00000000000000000000000000000000"	19337
VHDL info at dspba_library.vhd(76): executing entity "dspba_delay(width=42,reset_kind="SYNC")(1,4)" with architecture	19337
VHDL info at dspba_library.vhd(17): executing entity "dspba_reg(width=42,init_value="00000000000000000000000000000000"	19337
VHDL info at fft1k_pe_reset_in.vhd(9): executing entity "fft1k_pe_reset_in" with architecture "rtl"	19337

System Processing (38)

13% 00:00:13



# Compiled Resource Summary

The screenshot displays the Quartus Prime Pro Edition interface. The main window shows the 'Flow Summary' for a compilation report. The 'Table of Contents' on the left lists various sections, with 'Flow Summary' selected. The 'Flow Summary' pane on the right provides a detailed overview of the compilation process, including the flow status, version information, and a comprehensive list of resource utilization statistics.

**Flow Summary**

Flow Status	Successful - Wed Jul 28 11:55:00 2021
Quartus Prime Version	21.1.0 Build 169 03/24/2021 SC Pro Edition
Revision Name	unified_fft
Top-level Entity Name	unified_fft
Family	Agilex
Device	AGFB014R24B2E2V
Timing Models	Preliminary
Power Models	Preliminary
Device Status	Preliminary
Logic utilization (in ALMs)	5,273 / 487,200 ( 1 % )
Total dedicated logic registers	8995
Total pins	114 / 924 ( 12 % )
Total block memory bits	2,662,748 / 145,612,800 ( 2 % )
Total RAM Blocks	151 / 7,110 ( 2 % )
Total DSP Blocks	26 / 4,510 ( < 1 % )
Total eSRAMs	0 / 2 ( 0 % )
Total HSSI P-Tiles	0 / 1 ( 0 % )
Total HSSI E-Tile Channels	0 / 24 ( 0 % )
Total HSSI HPS	0 / 1 ( 0 % )
Total HSSI EHIPS	0 / 4 ( 0 % )
Total PLLs	0 / 24 ( 0 % )

The bottom of the interface shows a 'Messages' pane with the following content:

```
System (5) Processing
(5) (0) (0) (0) (0)
Loading final database.
Successfully loaded final database: elapsed time is 00:00:00.
Loading final database.
Loading "final" snapshot for partition "root_partition".
Successfully loaded final database: elapsed time is 00:00:00.
```



# Timing Analyzer report

Timing Analyzer - /data/projects/OneAPI/Q\_projects/FFT/AGILEX/fft64k\_d16\_c16\_v2/unified\_FFT\_2...

File View Netlist Constraints Reports Script Tools Window Help Search Intel FPGA

Set Operating Conditions Snapshot: final

- ✓ Slow vid2 100C Model
- ✓ Slow vid2a 100C Model
- ✓ Slow vid2b 100C Model
- ✓ Fast vid2a 0C Model

Report

- SDC File List
- Setup Summary
- Fmax Summary**

Tasks

- ✓ Open Project...
- Netlist Setup
- ✓ Create Timing Netlist

**Fmax Summary**

Show: Visible

	Fmax	Restricted Fmax	Clock Name	
1	642.26 MHz	500.0 MHz	clock_in_in_clk_clk	limit due to minimum

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Intel recommends that you always use clock constraints and other slack reports for sign-off analysis.

Deriving Clocks

- No user constrained clock uncertainty found in the design. Calling "derive\_clock\_uncertainty" will report the clock uncertainty characteristics of the device.
- Clock uncertainty characteristics of the Agilex device family are preliminary
- Deriving Clock Uncertainty. Please refer to report\_sdc in the Timing Analyzer to see the details.

qsta\_utility::auto\_report\_setup

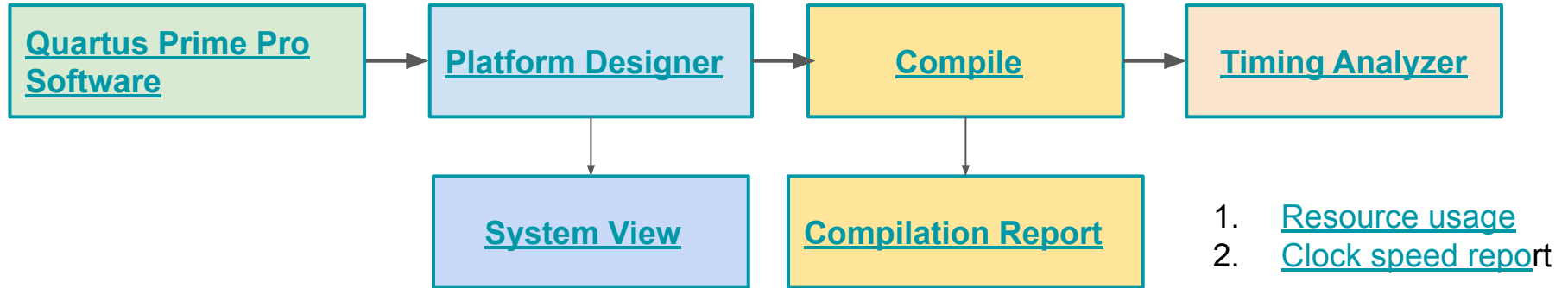
Console History

Ready



# Performance Tests of Agilex FPGA Using VHDL

## Quartus design flow



FFT IP  
1 k to 64 k point



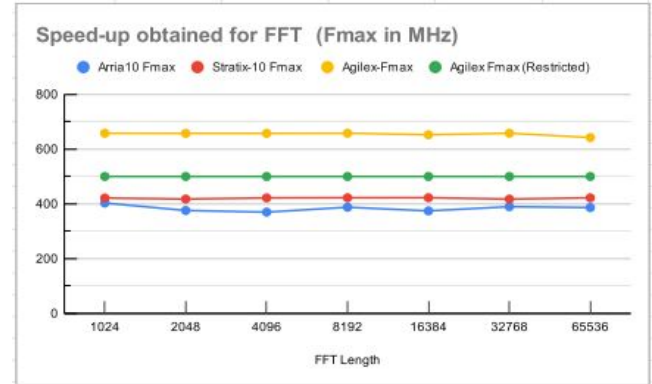
# Results

QUARTUS : 21.1		IP Used : FFT Intel FPGA IP						
DEVICE : Agilex: AGFB014R24B2E2V		Core Speed : 2						
Sl. No	Design Name	FFT Length	ALM (487,200)	Block Mem(145,612,800)	RAM (7,110)	DSP (4,510)	Restricted Fmax (MHz)	Fmax ( MHz)
1	fft1k_d16_c16	1024	2,365	35,480	7	14	500	657.89
2	fft2k_d16_c16	2048	2,519	80,226	11	18	500	657.46
3	fft4k_d16_c16	4096	2,841	161,804	15	18	500	657.46
4	fft8k_d16_c16	8192	3,317	331,480	24	22	500	657.89
5	fft16k_d16_c16	16384	3,654	666,756	46	22	500	652.32
6	fft32k_d16_c16	32768	4,504	1,345,716	81	26	500	657.89
7	fft64k_d16_c16	65536	5,273	2,662,748	151	26	500	642.26
DEVICE : Stratix 10: 1SG280LN2F43E2VG		Core Speed : 2						
Sl. No	Design Name	FFT Length	ALM (933,120)	Block Mem(240,046,080)	RAM (11,721)	DSP (5,760)	Restricted Fmax (MHz)	Fmax ( MHz)
1	fft1k_d16_c16	1024	1,712	35,328	7	14	421.41	421.41
2	fft2k_d16_c16	2048	1,910	79,956	11	18	417.54	417.54
3	fft4k_d16_c16	4096	2,125	161,564	15	18	421.76	421.76
4	fft8k_d16_c16	8192	2,488	331,160	24	22	422.3	422.3
5	fft16k_d16_c16	16384	2,723	666,428	45	22	422.48	422.48
6	fft32k_d16_c16	32768	3,218	1,345,270	79	26	417.36	417.36
7	fft64k_d16_c16	65536	3,725	2,662,246	150	26	422.12	422.12
DEVICE : Arria 10: 10AX115H3F34I2SG		Core Speed : 2						
Sl. No	Design Name	FFT Length	ALM (427,200)	Block Mem(55,562,240)	RAM (2,713)	DSP (1,518)	Restricted Fmax (MHz)	Fmax ( MHz)
1	fft1k_d16_c16	1024	1,450	38,224	9	14	403.06	403.06
2	fft2k_d16_c16	2048	1,664	80,500	11	18	375.94	375.94
3	fft4k_d16_c16	4096	1,848	162,204	15	18	369.82	369.82
4	fft8k_d16_c16	8192	2,118	331,960	24	22	387.75	387.75
5	fft16k_d16_c16	16384	2,316	667,608	46	22	374.39	374.39
6	fft32k_d16_c16	32768	2,678	1,347,172	81	26	389.71	389.71
7	fft64k_d16_c16	65536	2,885	2,665,640	149	26	386.55	386.55

Agilex

Stratix-10

Arria-10



# Results

QUARTUS : 21.1

DEVICE : Agilex: AGFB014R24B2E2V

Sl. No	Design Name	FFT Len
1	fft1k_d16_c16	102
2	fft2k_d16_c16	204
3	fft4k_d16_c16	409
4	fft8k_d16_c16	819
5	fft16k_d16_c16	1638
6	fft32k_d16_c16	3276
7	fft64k_d16_c16	6553

Agilex

DEVICE : Stratix 10: 1SG280LN2F43E2VG

Sl. No	Design Name	FFT Len
1	fft1k_d16_c16	102
2	fft2k_d16_c16	204
3	fft4k_d16_c16	409
4	fft8k_d16_c16	819
5	fft16k_d16_c16	1638
6	fft32k_d16_c16	3276
7	fft64k_d16_c16	6553

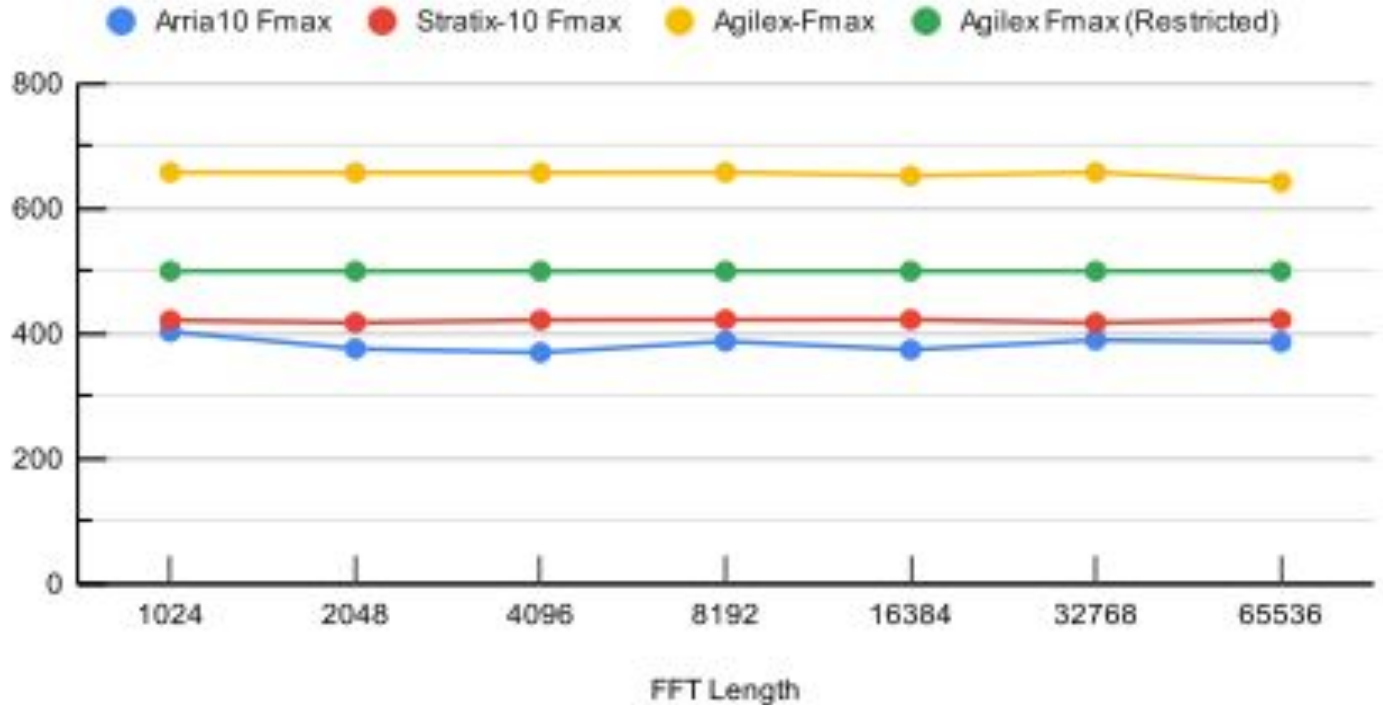
Stratix-10

DEVICE : Arria 10: 10AX115H3F34I2SG

Sl. No	Design Name	FFT Len
1	fft1k_d16_c16	102
2	fft2k_d16_c16	204
3	fft4k_d16_c16	409
4	fft8k_d16_c16	819
5	fft16k_d16_c16	1638
6	fft32k_d16_c16	3276
7	fft64k_d16_c16	6553

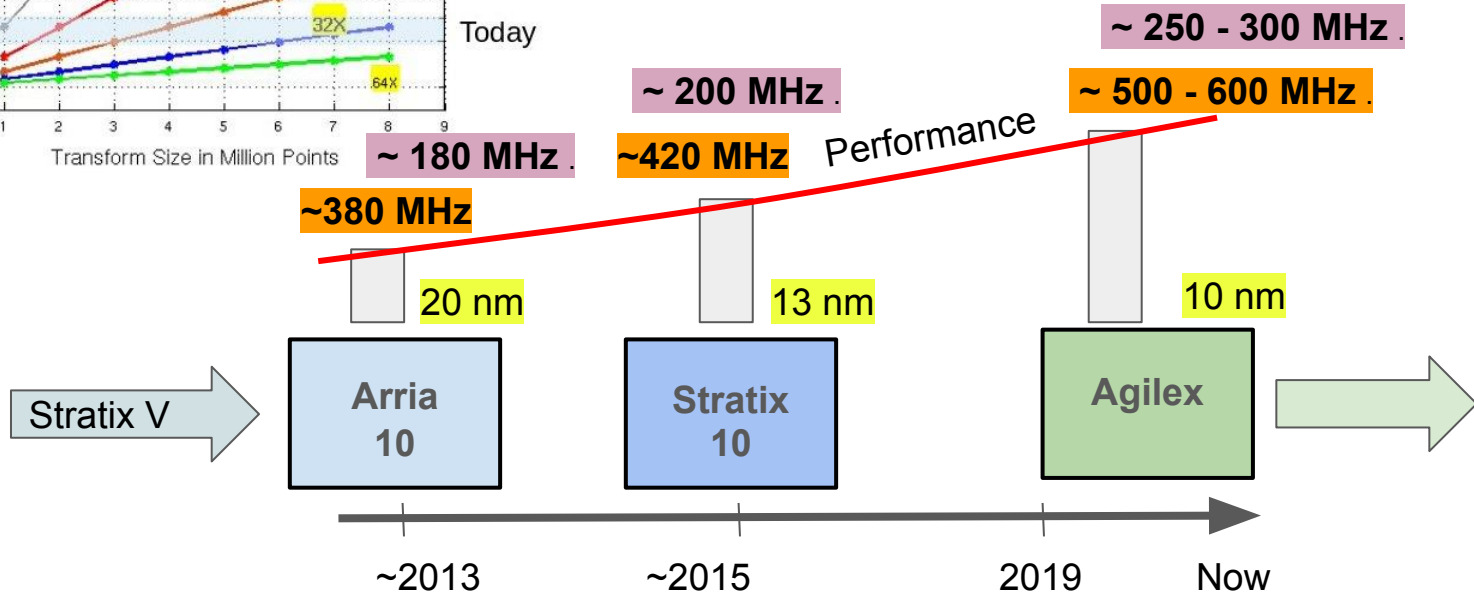
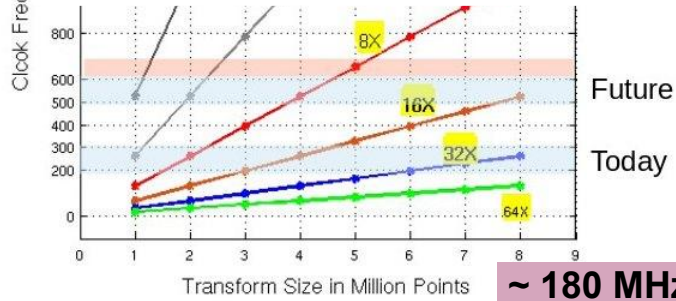
Arria-10

## Speed-up obtained for FFT (Fmax in MHz)





Results match with our pre 2017 projection for the FPGA acceleration



**THANK YOU**