Concluding Report
AT4-505, -506, -507, -510 and -511
SPO-1191 New FPGA Development Environments

Contributors: P. Thiagaraj, C. Vinutha

August 2021

1 Introduction

The objective for this study is to research new generation FPGA capabilities and their development environments. PSS modules have VHDL and OpenCL implementations for FPGA based acceleration. OneAPI is a recent move from intel to provide a familiar C++ development environment across heterogeneous accelerators: FPGA, GPU and CPU. It is based on SYCL, provides a uniform host-accelerator interface and development tools. The latest FPGA accelerators are on the horizon, and their development environments are changing to provide better efficiency. This study evaluates this emerging landscape and reassesses the acceleration capabilities of the FPGA based accelerators.

We have carried out four different studies and separately documented the findings from each study.

- Setting up an OneAPI Environment
- Study on OneAPI tool flow
- Running VHDL from OpenCL and OneAPI
- FPGA Speedup study - How fast is Agilex?
- Follow up plans

At the end of it, we have also identified a few follow-up tasks. This report gives a consolidated account of this landscape study.

2 Setting up OneAPI Environment

At first, we made a preliminary study to understand the OneAPI environment, learned about the concepts behind OneAPI Data-Parallel C++ and system requirements to install and run the OneAPI tools. After the survey, we successfully set up the OneAPI environment in a local AMD server running Ubuntu 20.04 and executed a few test codes. A report of this work was produced [1].

3 Study on OneAPI tool flow

This study examines the OneAPI code compilation, execution, and debugging tools. We have used example DPC++ codes from intel to verify the tools. We successfully compiled and executed a few example codes on CPU and in FPGA emulation modes. We have also successfully investigated the use of gdb based OneAPI debugging tool. The use and the limitations of the DPC++ code performance analysis tool Intel's VTune were studied. We have also observed that the SYCL based code development is available for NVIDIA GPUs and XILINX FPGAs. A report of this work was produced [2].

4 Running VHDL from OpenCL and OneAPI

This study investigated the procedure used to run VHDL codes from OneAPI, and OpenCL tool flow and the findings are documented [3]. We also found discrepancies in the library creation procedure recommended by intel and following with intel to sort them out.

5 FPGA Speedup study - How fast is Agilex?

This work is about a study on the performance of Agilex FPGA compared to the previous generation FPGAs. We have chosen Arria-10, launched around in 2013, Stratix-10 in 2015 and Agilex in 2019. These FPGAs belong to three generations, with their VLSI technology being 20, 13 and 10 nm. Correspondingly their speed performance is also anticipated to be progressively better. To Analyze, we have used FFT IP cores of varying complexity and synthesized the design for a mid-speed grade, mid-size Agilex FPGA using the intel Quartus 21.1 software. The FFT IP length varied from 1k to 64k points for the analysis. FPGA resource usages and clock performances were tabulated to analyze the improvements observed between the three FPGAs.

In summary, we ascertained the speed performance available with the current generation FPGA that match our anticipated performance from 2017. We expect to achieve clock throughputs up to half the maximum reported when the FPGA contains the whole design. This study was beneficial for the PSS accelerator scaling. The results from this work were documented and demoed [4][5].

6 Follow up plans

Based on this study, we have specific follow up tasks identified:

- FPGA emulation versus hardware execution.
- Executing VHDL from OneAPI
- Enhancing the emulator mode
- Use of VTune on non-Intel CPUs
- OneAPI across FPGA and GPU
- Agilex Accelerators with OneAPI

6.1 FPGA emulation versus hardware execution.

FPGA emulation mode Versus hardware. Currently, we have executed the OneAPI FPGA codes in an emulation mode. We have installed and used the latest 2021 version of OneAPI for these studies. Intel's OneAPI for the gx10 FPGA card is available from an earlier (2018) version of Quartus. We have identified a task to sort this issue and evaluate the hardware execution of the OneAPI. version 18.x versus 21.x

6.2 Executing VHDL from OneAPI

The library object creation procedure needs an object-manifest XML file to be supplied by the user. Currently, the documents section suggests a standard guideline for this between OpenCL and OneAPI. We have observed an incompatibility issue here with the OneAPI $\text{fpga}_c rossgentoolflow.Wearefollowingthematterupwithintel.$

6.3 Enhancing the emulation mode

The VHDL study provided insight into the emulation mode for an FPGA. We have a better understanding of how to incorporate efficient C-models for a design. This feature will be helpful to provide alternate high-performance heterogeneous execution options.

Use of VTune on non-Intel CPUs Our OneAPI server is based on AMD CPU, and the VTune tool could not provide feedback to optimise CPU performance. We are looking into better understand the issue and its implications for non-Intel CPUs running OneAPI.

6.4 Agilex Accelerators with OneAPI

Multiple vendors have announced the next generation of FPGA accelerators. We made a preliminary study and found that many of them will support OneAPI for the FPGA acceleration. We learn that Terasic, Bittware and Intel will have OneAPI releases for their respective accelerators in the next few months. Appendix-A presents the cards announced by these vendors where we expect the OneAPI support in 2021.

7 Conclusion

We have investigated the following in this work:

- Philosophy behind the DPC++/OneAPI
- DPC++ and SYCL framework
- Example code execution on CPU and FPGA emulation
- Compilation tool
- Debugging procedure/tool
- Code performance analysis
- procedure for including VHDL in OneAPI
- Speed up study for FPGAs

OneAPI DPC++ is a better-evolved concept than the OpenCL. The main advantage comes from conveniences with testing, debugging and maintaining the accelerator codes as they now form a single entity along with the host code. The current implementation of OneAPI is likely to change due to the fact that SYCL has a new version and also due to the new generation FPGA accelerators coming soon.

This feature helped us assess the latest FPGA performances and use of their development environments for the PSS. We propose taking a few focused tasks to follow up with the updates from the tool flow releases and the new accelerators.

—x—

A Appendix

Agilex FPGA accelerators from three different vendors are shown in Fig. 1 to 3. these cards are expected to have the OneAPI environment. There are also other vendors bringing the Agilex accelerators to the market soon, and we are also following them up.

Figure 1: Terasic Agilex Accelerator: DE10 - https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=142&No=1252

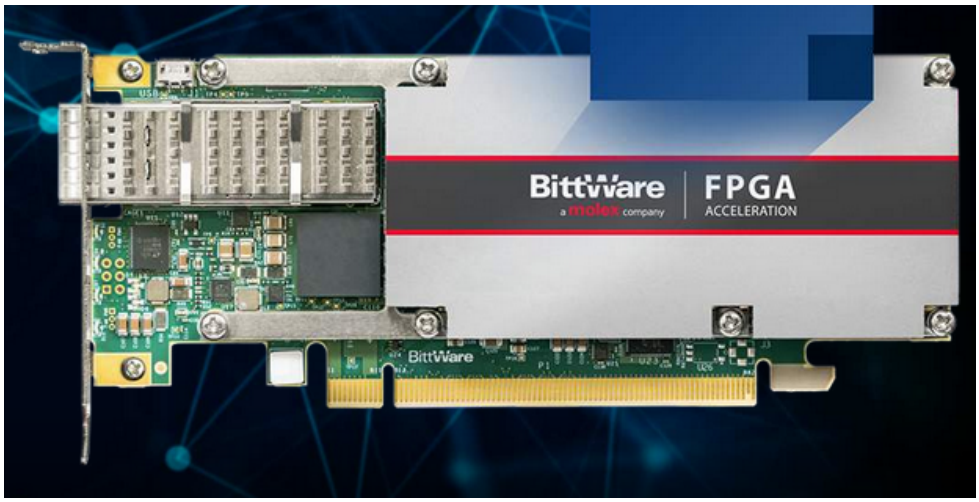

Figure 2: Bittware Agilex ccelerator: IA-420F - https://www.bittware.com/fpga/ia-420f/

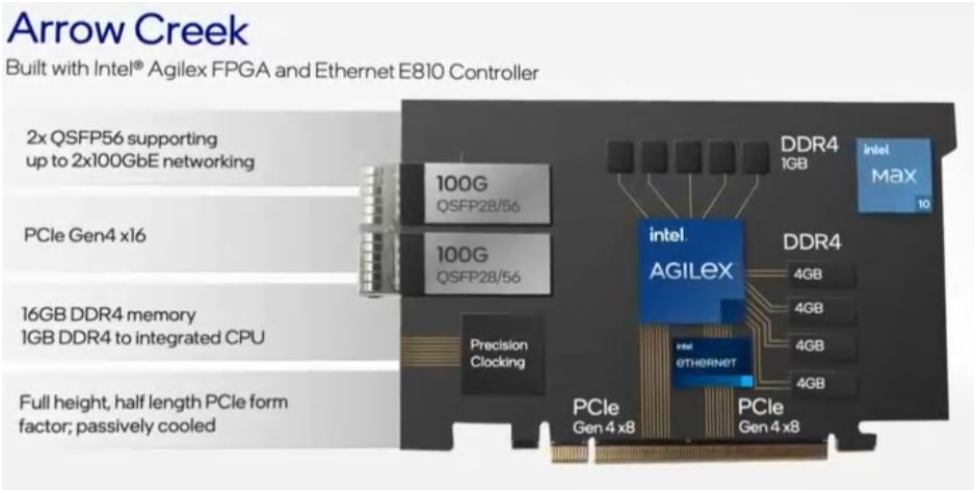

Figure 3: Intel's Agilex Accelerator: Arrow creek - https://www.servethehome.com/wp-content/uploads/2021/08/Intel-Architecture-Day-2021-IPU-Arrow-Creek-2.jpg

B References

1. Setting up an OneAPI Environment https://docs.google.com/document/d/19_B6HJKFSaEDZyBn2upgHpo-H_THjQpe3r_cHOia2Vw/edit?usp=sharing

2. Comparison of tool flow: AT4-507 Comparison of Compilation, Execution,Debugging flows between oneAPI and OpenCL. - https://drive.google.com/file/d/18eoq0mSqkYiulqJTcIEwAXi0oEAKN669/view?usp=sharing

3. VHDL, OpenCL and OneAPI - https://drive.google.com/file/d/1Xb3Lw1HRc-APii2tMD-CzXe1Ze0yScen/view?usp=sharing

4. FPGA Speedup study - report - https://drive.google.com/file/d/1WfZnnQtytYwTpbbg5aOenD3bXpgaUJUY/view?usp=sharing

5. FPGA Speedup study - Demo - https://drive.google.com/file/d/14hu9ubpiCNMYd4ryh9NHjpClInXUyajZ/view?usp=sharing

6. Pre2017 report https://drive.google.com/file/d/1TaF57PRCXs-tEGCI3trXmEi3vIEwjrRW/view?usp=sharing