Pulsar Timing (PST) Channelizer - 4096 Channel Output (PSTC_CH4K)

The Pulsar Timing (PST) Channelizer (PSTC_CH4K) firmware block is used to segment the Frequency Slices (FSs) into 4096 channels [MD] - section 5.6. This firmware block is to be first used in the Talon Demonstrator Correlator (TDC) and subsequently in the Square Kilometre Array (SKA) Mid Correlator Beamformer (Mid.CBF). The PSTC_CH4K is implemented using the architecture of a oversampled polyphase DFT filter-bank (OSPPFB) [MD] - section 4.3.4.1.

[MD] SKA1 CSP Mid Array Correlator and Central Beamformer Sub-element Signal Processing MATLAB Model (EB-7), V4, 2018-08-16.

Functional Behavior

The segmentation of the input spectrum with a OSPPFB having Nch output channels is shown in Figure 1. Note that unlike the IC_CH16K, PSTC_CH4K channels are non-overlapped and thereby allow recovery of the original spectrum within an arbitrary accuracy.

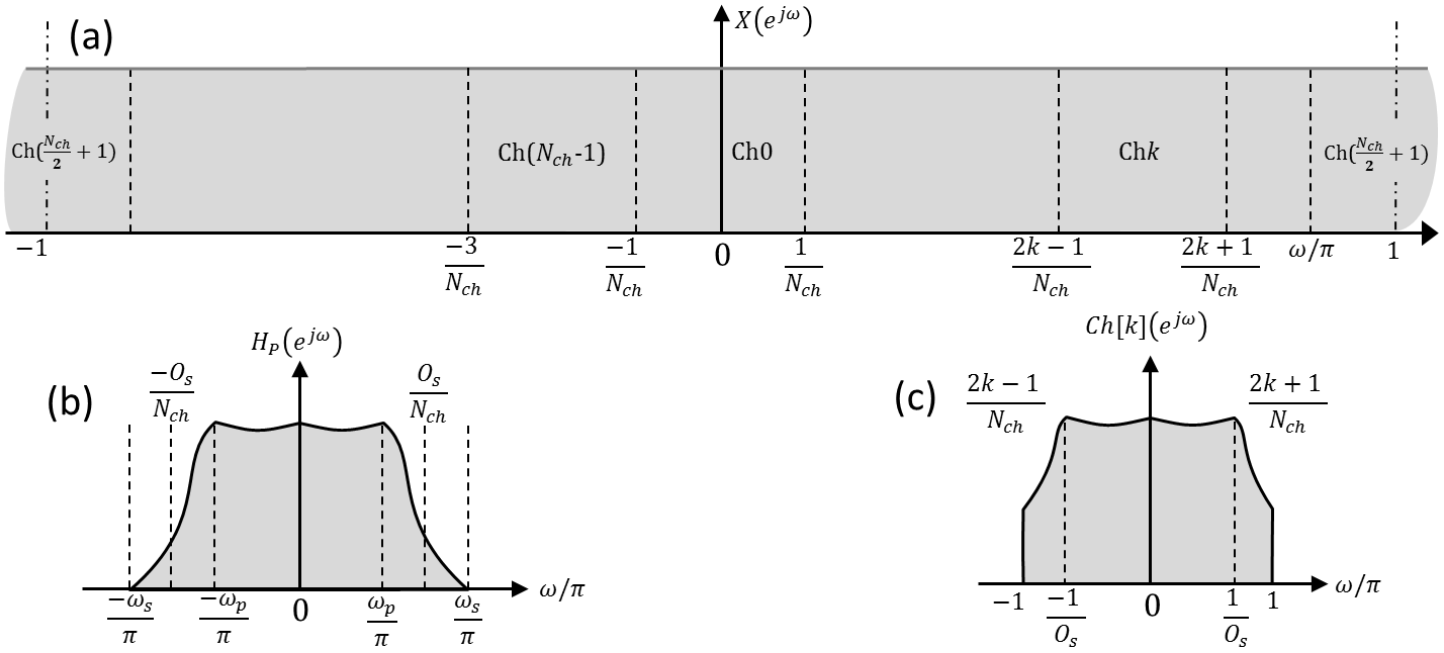

Figure 1. The segmentation of the input spectrum with a OSPPFB. (a) The input spectrum and the boundaries of the channels. (b) The magnitude transfer function of the prototype filter. (c) The magnitude response of any channel.

The agreements among the ideal response, MATLAB and the SIMULINK implementations of a PSTC_CH4K are shown in Figure 2.

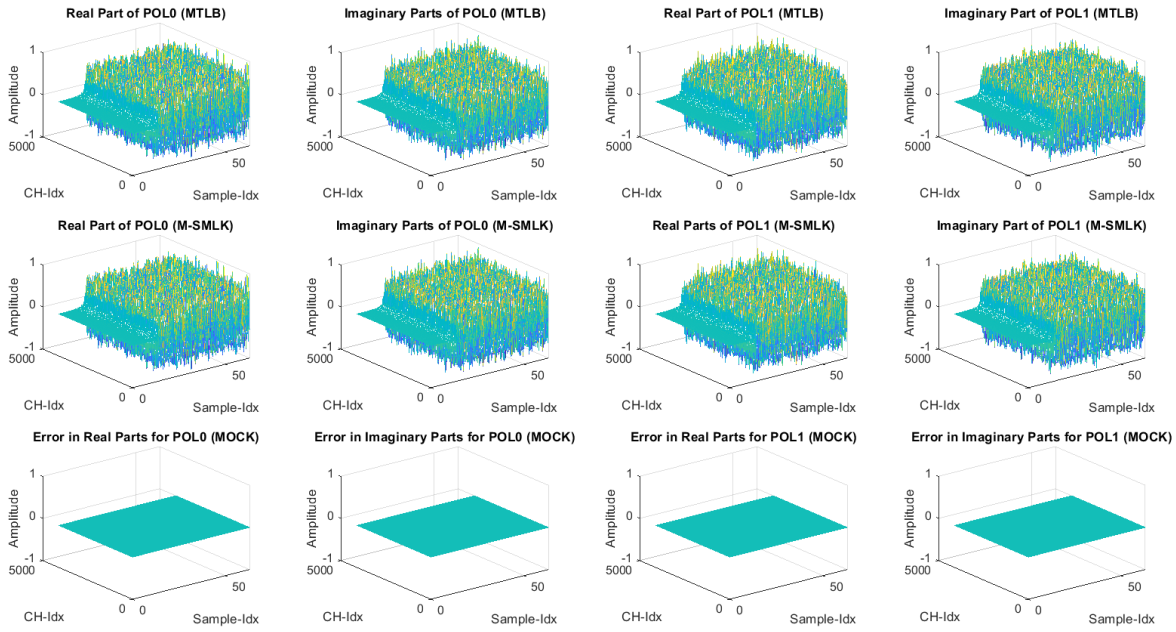

Figure 2. Agreements among the ideal response, MATLAB and the SIMULINK implementations of the PSTC_CH4K for the two polarization components.

Firmware Interface

The block diagram of the PSTC_CH4K firmware block is shown in Figure 3.

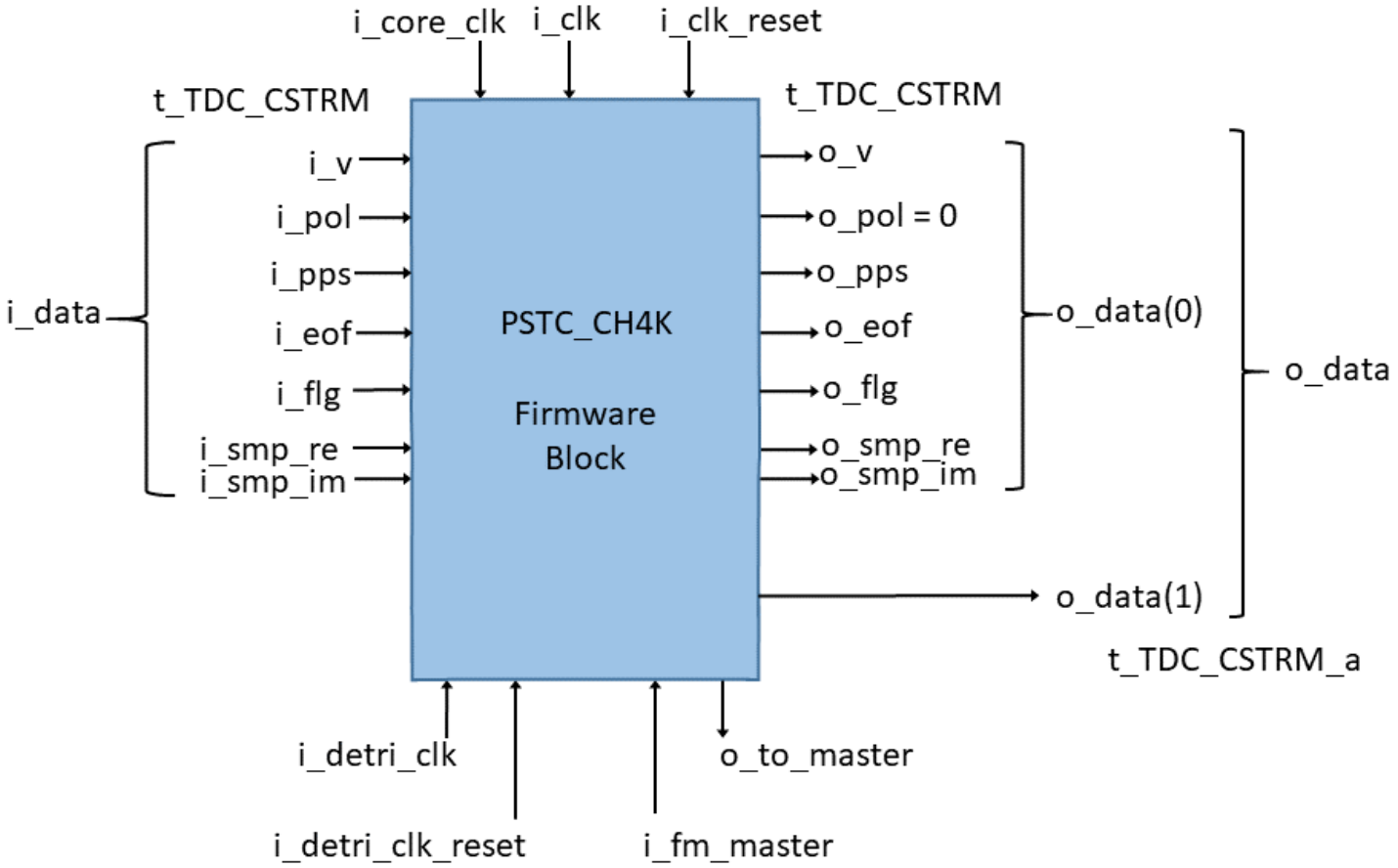

Figure 3. The block diagram of the PSTC_CH4K firmware block.

```
entity pstc_ch4k is

generic(
  g_IP_PPS_SAMPLE_COUNT  : integer := 220200960; --The number of samples between PPS markers at th
                           --NOTE This value must be an integer multiple of 3584
  g_INTERCONNECT_PARAMS  : t_detri_interconnect_parameters
);

port(
   -- DeTrI interface
   i_detri_clk       : in std_logic;
   i_detri_clk_rst   : in std_logic;
   i_fm_master       : in t_DETRI_MOSI;
   o_to_master       : out t_DETRI_SOMI := c_DETRI_SOMI_DEFAULT;

   -- Input Datapath Clock / Reset
   i_clk             : in std_logic;  -- @ 450 MHz
   i_clk_rst         : in std_logic;

  -- Input Clock that Runs the Core of the Firmware block
  i_core_clk        : in  std_logic; -- @ 270 MHz
```

```
    -- Ingress Interface
    -- A single Frequency Slice with time multiplexed polarization components.
    i_data            : in t_CPLX_STRM;

    -- Egress Interface
    -- 4096 Pulsar Timing Channels in series for a single polarization component.
   -- The two polarizations are arranged in two streams.
    o_data            : out t_CPLX_STRM_a(0 to 1)

  );
end entity pstc_ch4k;
```

INPUTS

- The clock input for internal signal processing and output is 'i_core_clk'
- The clock input is 'i_clk'.
- The reset input 'i_clk_reset' is active high and should be held at least 256 clock cycles.
- The input data 'i_data' is a record containing (18+18)-bit wide complex-valued data, time markers, polarization marker, valid and flags are bundled in the record of type 't_CPLX_STRM' defined in dsp_lib. The 'i_data' record is consisted of,
- The 'i_v' input marks valid inputs frames and is used for the input flow control (i.e. input throttling).
- The 'i_pol' input marks the polarization id of the time-multiplexed input sequence.
- The 1PPS (pulse per second) marker for the input sequences is marked by the 'i_pps'. Note that the 1PPS for POL0 precedes the 1PPS for POL1 and asserted in adjacent valid cycles.
- The end of frame marker 'i_eof' marks the valid samples before the 1PPS markers for both polarizations.
- The 'i_flg' marks all *flagged* (i.e. saturated, un-known) samples.
- The 'i_smp' is a record containing (18+18)-bit wide complex-valued data encoded in two's complement format.
- The DeTrl control interface clock input is 'i_detri_clk'.
- The DeTrl control interface reset input is 'i_detri_clk_reset'.
- The DeTrl control interface address, handshake and data inputs are bundled in the record 'i_fm_master'.

OUTPUTS

- The output 'o_data' is a record of type 't_CPLX_STRM_a' that contain two polarization components arranged in records of type 't_CPLX_STRM'. For each polarization component there are 4096 Pulsar Timing Channels (PSTCs) arranged in series in the *natural order*.

- For the polarization component 0 (POL0), 't_CPLX_STRM_a(0)' and polarization component 1 (POL1), 't_CPLX_STRM_a(1)'
- The output 'o_v' marks valid output sample-frames. These outputs are registered.
- The output 'o_pol' marks the id of the polarization component, i.e. '0' for POL0 and '1' for POL1 .
- The PPS markers for the output sequence is marked by the 'o_pps'. Note that 'o_pps' is asserted for all PSTCs corresponding to the same time instant in the corresponding frame.
- The output 'o_eof' marks the channel 4095.
- The output 'o_flg' indicate the *flagged* (i.e. saturated, un-known) samples.
- The complex-valued output samples [o_smp_re, o_smp_im] are represented in (18+18)-bit wide samples encoded in the two's complement format. Note that the least signaificant (2+2)-bits are set to zero and only the most significant (16+16)-bits carry the signal.
- The DeTrI control interface handshake and data outputs are bundled in the record 'o_to_master'.

PARAMETERS

- For the two polarization components of the Ny=4096 PSTCs, individual bit-shift are applied scaling up or down the magnitude of the PSTCs by factors of 2^n. The bit-shifts are represented as unsigned integers and stored in the Memory-Mapped registers {PSTC_shift_P0[0,...,(Ny-1)]} and {PSTC_shift_P1[0,...,(Ny-1)]}, which are 4-bits wide. These registers are updated through the DeTrI interface.
- For the two polarization components of the Ny=4096 PSTCs, individual scaling-factors are applied to scale down the magnitude of the PSTCs. The scaling-factors are represented as singed integers and stored in the Memory-Mapped registers {PSTC_scale_P0[0,...,(Ny-1)]} and {PSTC_scale_P1[0,...,(Ny-1)]} , which are 16-bits wide. These registers are updated through the DeTrI interface.

CRITERIA FOR ASSERTION OF FLAGS

- 'o_flg' is asserted and 'o_v' is de-asserted for both Pol samples until the first PPS marker arrives.
- 'o_flg' is asserted for samples of both Pols for the first 29 valid outputs indicating partially filled input data pipeline.
- If 'i_flg' is asserted, 'o_flg' is asserted for the next 29 valid outputs for the corresponding Pol indicating contaminated outputs.
- If there is a slip/miss of the PPS markers (i.e. there should be nominal number of valid samples between the PPS) after the initial PPS arrived, 'o_flg' is asserted for the corresponding Pol samples until 'pstc_ch4k' sees the expected number of valid sample between consecutive PPS markers.
- If the 'Rate Matching FIFO' get filled, 'o_flg' is asserted for the next 29 valid outputs. This would lead to non-nominal number of samples between PSS markers and therefore, 'o_flg' would be asserted for the following one second.

- 'o_flg' is asserted for individual samples, if the 'o_smp' saturate when re-quantize to [16+16]-bits, after shifting/scaling.

GENARAL FACTS

- The input signal is delivered with a clock at 450 MHz. The internal signal processing is carried out at 270 MHz. The two output streams are delivered with a clock at 270 MHz.

TEST SCENARIOS

There are three types of testing performed during the development stage. The firmware block has been simulated in ModelSim using the test vectors generated with MATLAB/SIMULINK. The outputs of the 'pstc_ch4k' firmware block has been compared against the outputs evaluated with MATLAB/SIMULINK. Output signals 'o_pol', 'o_pps', 'o_eof', 'o_flg' need to be matching exactly for each valid output sample to pass the test. Similarly, the output samples 'o_smp_re' and 'o_smp_im' for both polarization components need to remain within the final quantization step (3.0517578125-05) for each valid output sample to pass the test.

- T001.
  Tests the basic signal processing functionality along with flagging for partially filled signal processing pipeline and saturation. Scaled Gaussian inputs are used as the input test vectors. The corresponding outputs are shown in Figure 4.

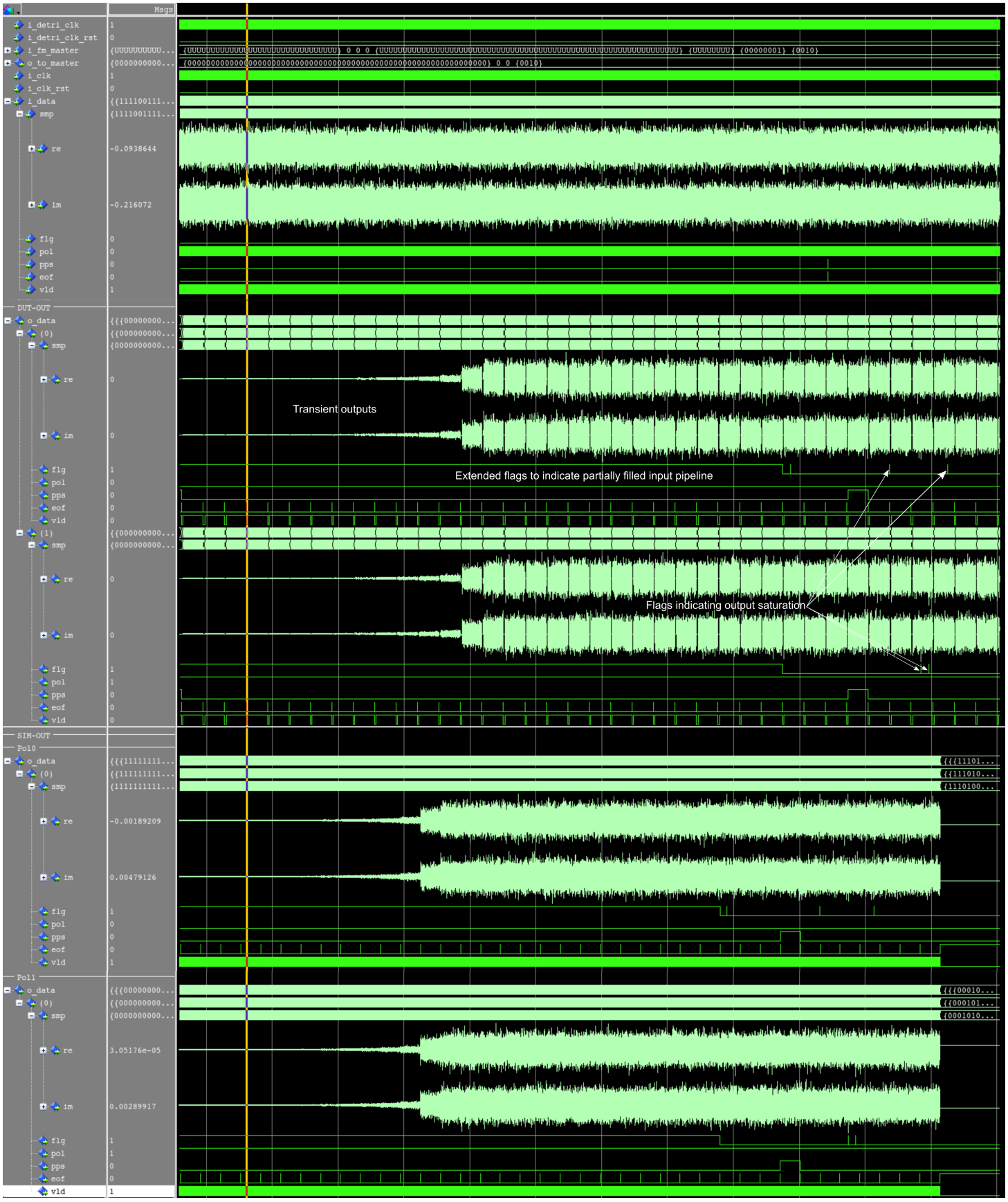

Figure 4. The simulated outputs for Gaussian inputs that verifies the general singal processing functionality.

- T002.
  Tests the flagging for partially filled signal processing pipeline and extension of input flags. For both

polarizations, unit impulse is used to marks the location of the input flag in the input sequence. The convolution spread of the contaminated sample is shown in Figure 5.

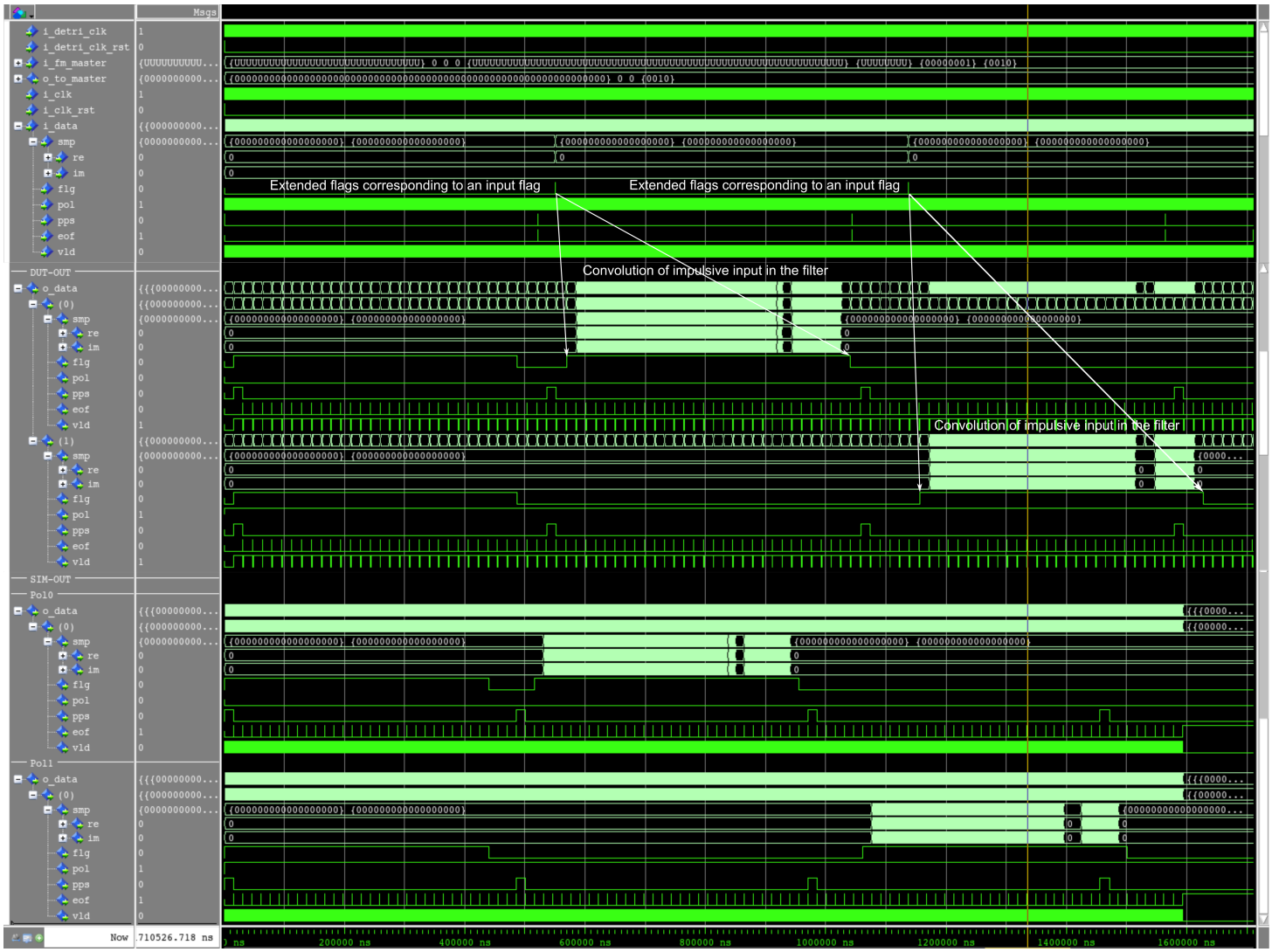

Figure 5. The simulated outputs for impulsive inputs that coincide with input flags to verify the flag extension.

- T003.
  Tests the change of shifting and scaling factors using the DeTri interface. The test vectors are generated using a combination of sinusoids of different amplitudes and phases. The shifting and scaling factors either enhance or suppress output magnitude of the specific channels containing the sinusoids. For the case shown in Figure 6, the input is synthesized with 16 sinusoids having amplitudes spanning 50 dB. The frequencies of the sinusoids span [-0.9, 0.9] in normalized frequency range. The corresponding channel indices are calculated and the shifting factors for these channels have been selected to scale back the magnitudes of the corresponding channels within unity. The associated scaling factors are selected randomly to be in the range [0.795, 0.995].

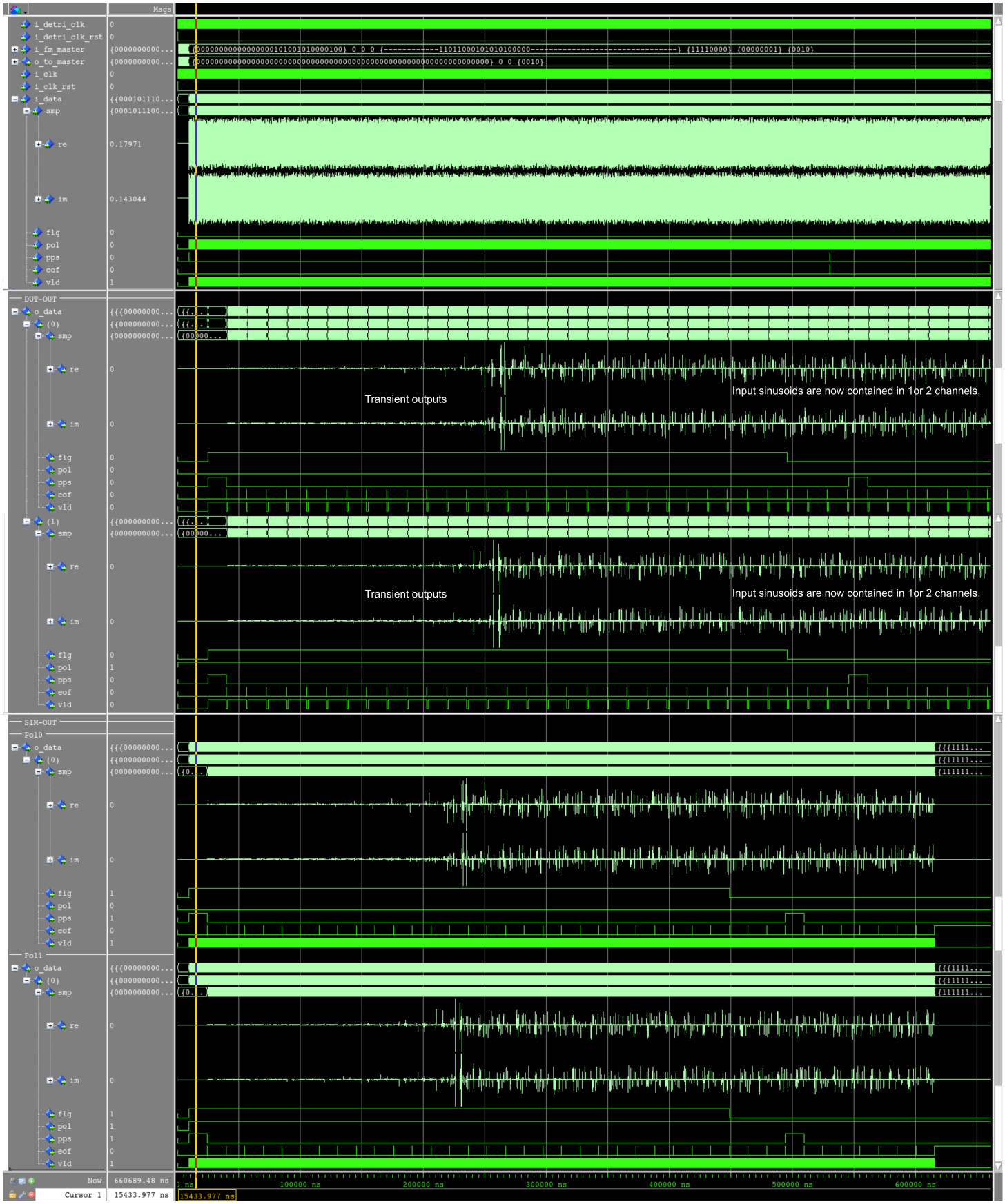

Figure 6. The simulated outputs for combined sinusoids that verifies the shifting and scaling factors are applied correctly.