Product Specification
12x25G On-Board Transceiver

CONFIDENTIAL DOCUMENT

Preliminary Version

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General Description

The Onboard Transceiver (OBT) is an electrically and optically pluggable device.
The receiving side of the Transceiver Module comprises a 12 Channel Transimpedance / Limiting Amplifier (TIA/LIA). Through the Optical Port, the PIN diode array, in combination with the TIA/LIA, the incoming parallel optical data signals are converted into a parallel stream of outgoing electrical data signals.
The transmitting side of the Transceiver Module comprises a 12 Channel Driver. The parallel electrical signals from the HOST board modulate a 850nm VCSEL laser array which, in turn, generates parallel optical data signals to be launched into a fiber cable via the Optical Port of the OBT.

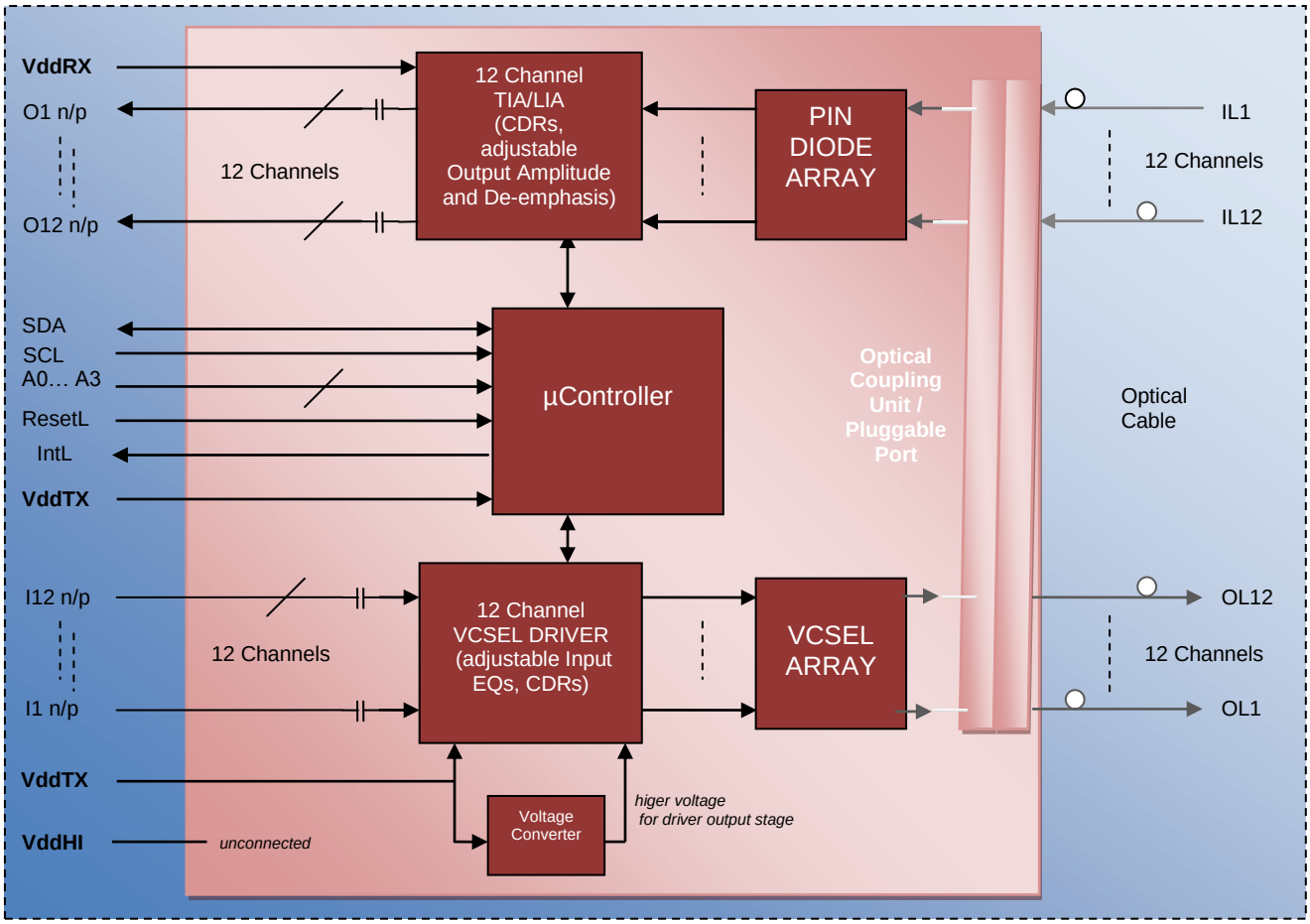


Figure 1 OBT Transceiver

An I^2C serial interface (SDA, SCL) allows access to various controls and status registers of the transceiver.

Each receiver output supports individual output voltage swing and de-emphasis. This allows individual compensation of high frequency losses of the electrical data paths from the transceiver to the host system receiver. The control of the de-emphasis is accessible via the serial interface (see Receiver Voltage Output Swing and Emphasis Setting).

Each transmitter input supports individual input signal equalization. This allows individual compensation of high frequency loss of the electrical data paths from the host system transmitter to the transceiver. The control of the equalization is accessible via the serial interface (see Input Equalizer).

For the receive as well as transmit side, a CDR can be enabled per lane.

Nomenclature

The physical electrical and optical lanes and contact pins will be count from 1 to 12 eg. TxChannel 1 or TxCDR 12 for this product.

However, all register bits and its register names will be count from 0 to 11.

Electrical Pad Layout

0	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	GND	VDDTX	VDDTX	SCL	SDA	VDDHI	DNC	DNC	DNC	ResetL	IntL	VDDRX	VDDRX	GND	GND
2	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
3	GND	I2N	I2	GND	I1N	I1	GND	DNC	GND	O1	O1N	GND	O2	O2N	GND
4	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
5	GND	I4N	I4	GND	I3N	I3	GND	DNC	GND	O3	O3N	GND	O4	O4N	GND
6	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
7	GND	I6N	I6	GND	I5N	I5	GND	DNC	GND	O5	O5N	GND	O6	O6N	GND
8	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
9	GND	I8N	I8	GND	I7N	I7	GND	DNC	GND	O7	O7N	GND	O8	O8N	GND
10	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
11	GND	I10N	I10	GND	I9N	I9	GND	DNC	GND	O9	O9N	GND	O10	O10N	GND
12	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
13	GND	I12N	I12	GND	I11N	I11	GND	DNC	GND	O11	O11N	GND	O12	O12N	GND
14	GND	GND	GND	GND	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND
15	GND	VDDTX	VDDTX	SCL	SDA	VDDHI	A0	DNC	A1	A2	A3	VDDRX	VDDRX	GND	GND

Figure 2 Pad Layout (view through the transceiver on host board connector)

DNC = Do Not Connect. These pins are reserved. No signals shall be applied from HOST board to these pins.

PIN	Symbol	I/O	Description
F3,E3	I1, I1N	Input	TxChannel 1, Differential Transmitter Data Input, AC coupled
C3,B3	I2, I2N	Input	TxChannel 2, Differential Transmitter Data Input, AC coupled
F5,E5	I3, I3N	Input	TxChannel 3, Differential Transmitter Data Input, AC coupled
C5,B5	I4, I4N	Input	TxChannel 4, Differential Transmitter Data Input, AC coupled
F7,E7	I5, I5N	Input	TxChannel 5, Differential Transmitter Data Input, AC coupled
C7,B7	I6, I6N	Input	TxChannel 6, Differential Transmitter Data Input, AC coupled
F9,E9	I7, I7N	Input	TxChannel 7, Differential Transmitter Data Input, AC coupled
C9,B9	I8, I8N	Input	TxChannel 8, Differential Transmitter Data Input, AC coupled
F11,E11	I9, I9N	Input	TxChannel 9, Differential Transmitter Data Input, AC coupled
C11,B11	I10, I10N	Input	TxChannel 10, Differential Transmitter Data Input, AC coupled
F13,E13	I11, I11N	Input	TxChannel 11, Differential Transmitter Data Input, AC coupled
C13,B13	I12, I12N	Input	TxChannel 12, Differential Transmitter Data Input, AC coupled
A1 to A15	GND	Power	Common Ground
B2,B4,B6,B8,B10,B12,B14	GND	Power	Common Ground
C2,C4,C6,C8,C10,C12,C14	GND	Power	Common Ground
D2 to D14	GND	Power	Common Ground
E2,E4,E6,E8,E10,E12,E14	GND	Power	Common Ground
F2,F4,F6,F8,F10,F12,F14	GND	Power	Common Ground
G2 to G14	GND	Power	Common Ground
G1, H1 to H15,I1	DNC	(reserved)	Do not connect these pins on host board, reserved for OBT module
I2 to I14	GND	Power	Common Ground
J2,J4,J6,J8,J10,J12,J14	GND	Power	Common Ground
K2,K4,K6,K8,K10,K12,K14	GND	Power	Common Ground
L2 to L14	GND	Power	Common Ground
M2,M4,M6,M8,M10,M12,M14	GND	Power	Common Ground
N1,N2,N4,N6,N8,N10,N12,N14, N15	GND	Power	Common Ground
O1 to O15	GND	Power	Common Ground
B1,C1,B15,C15	VDDTX	Power	Power Supply Transmit Side
F1,F15	VDDHI	Power	not used, not connected inside OBT
L1,M1,L15,M15	VDDRX	Power	Power Supply Receiver Side
D1,D15	SCL	Input	I2C, Serial Clock, need Pull-up resistor on host board, see Table 13
E1,E15	SDA	Input/Output	I2C, Serial Data, need Pull-up resistor on host board, see Table 13
G15	A0	Input	I2C Address Line, internal 10k Pull-up resistor to VDDTX
I15	A1	Input	I2C Address Line, internal 10k Pull-up resistor to VDDTX
J15	A2	Input	I2C Address Line, internal 10k Pull-up resistor to VDDTX
K15	A3	Input	I2C Address Line, internal 10k Pull-up resistor to VDDTX
J1	ResetL	Input	Module Reset, internal 10k Pull-up resistor to VDDTX
K1	IntL	Output	Interrupt Low, need Pull up resistor on host board

PIN	Symbol	I/O	Description
J3,K3	O1, O1N	Output	RxChannel 1, Differential Receiver Data Output, AC coupled
M3,N3	O2, O2N	Output	RxChannel 2, Differential Receiver Data Output, AC coupled
J5,K5	O3, O3N	Output	RxChannel 3, Differential Receiver Data Output, AC coupled
M5,N5	O4, O4N	Output	RxChannel 4, Differential Receiver Data Output, AC coupled
J7,K7	O5, O5N	Output	RxChannel 5, Differential Receiver Data Output, AC coupled
M7,N7	O6, O6N	Output	RxChannel 6, Differential Receiver Data Output, AC coupled
J9,K9	O7, O7N	Output	RxChannel 7, Differential Receiver Data Output, AC coupled
M9,N9	O8, O8N	Output	RxChannel 8, Differential Receiver Data Output, AC coupled
J11,K11	O9, O9N	Output	RxChannel 9, Differential Receiver Data Output, AC coupled
M11,N11	O10, O10N	Output	RxChannel 10, Differential Receiver Data Output, AC coupled
J13,K13	O11, O11N	Output	RxChannel 11, Differential Receiver Data Output, AC coupled
M13,N13	O12, O12N	Output	RxChannel 12, Differential Receiver Data Output, AC coupled

Table 1

Electrical Hardware Pin Description

Power Supply (V_{DD}Tx, V_{DD}Rx, GND)
The OBT module has separate power supplies for Tx and Rx functions and a common ground.

The module comprises also an internal voltage converter, so external VddHI voltage is not required.
VddHI pins are unconnected inside module.

A0, A1, A2, A3
Address pins for the 2-wire interface. Internal connected with pull up resistor to V_{DD}TX.

ResetL Pin
ResetL has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up the module will post this completion of reset interrupt without requiring a reset.

IntL Pin
The OBT module has an independent active-low interrupt output pin. IntL is asserted when any unmasked interrupt alarm is set. The host may identify the specific interrupt alarm through the 2-wire interface. Reading the interrupt alarm will automatically clear the alarm and de-assert the IntL output. Note that IntL may not de-assert if the alarm is immediately reasserted due to an ongoing fault. The interrupt alarms may be masked by setting the associated registers.
The module initialization sequence occurs after a reset or power on. During the initialization sequence IntL is asserted and is automatically de-asserted once complete and indicates that the module is ready.
The IntL pin is an open collector output and must be pulled up to V_{DD}TX on the host board.

2-wire interface
Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface pins, SCL (clock), SDA (data).

Power Sequencing

There are no requirements for power sequencing of VddTx and VddRx.
VddHI is not used and unconnected inside OBT module.

CDR

TX CDR bypass / enable

As long as Global_TX_CDR bit is set to '0' all CDRs are bypassed.
By setting Bit 0 to '1' in Register 43 (0x2B) at TX Lower Page, all CDRs can be enabled.

However, it is possible to disable single CDR for one or more channels.
If single CDR needs to be bypassed, appropriated TX CDR Bit at Register 54 (0x36) and Register 55 (0x37) shall be set to '1'.

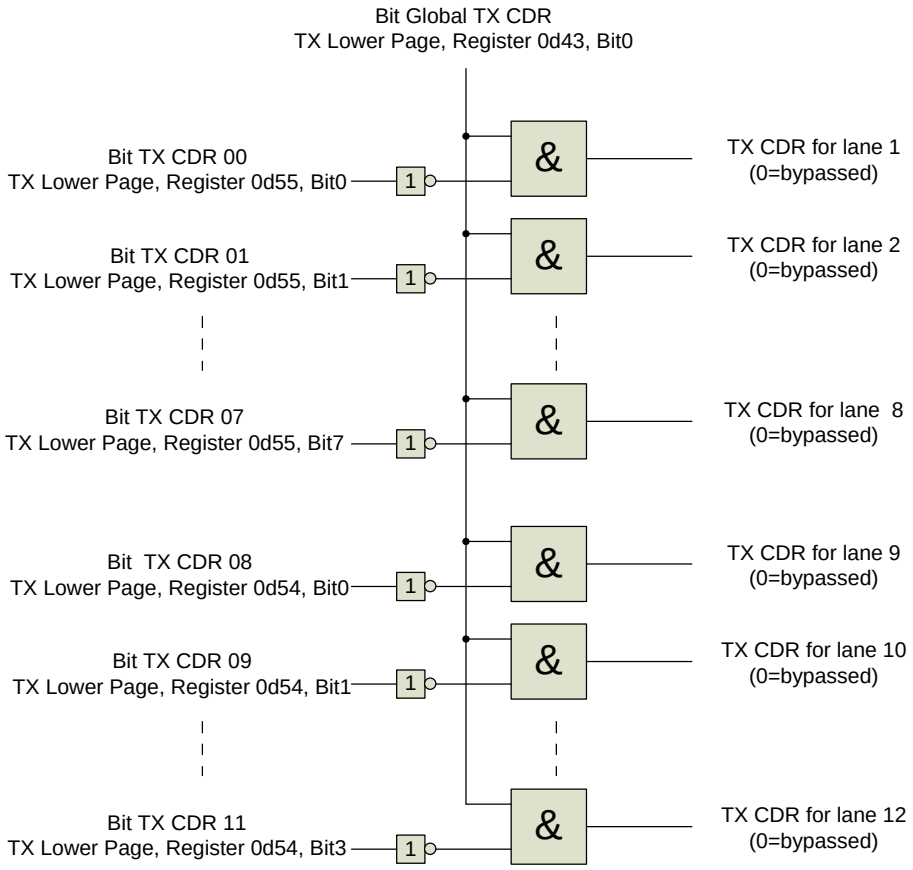


Figure 3 Tx CDR bypass

RX CDR bypass / enable

In analogy to the transmit side, RX CDR uses the same register definition like the TX CDR, but uses the RX Lower Page.

As long as Global_RX_CDR bit is set to '0' all CDRs are bypassed.
By setting Bit 0 to '1' in Register 43 (0x2B) at RX Lower Page, all CDRs can be enabled.

However, it is possible to disable single CDR for one or more channels.
If single CDR needs to be bypassed, appropriated RX CDR Bit at Register 54 (0x36) and Register 55 (0x37) shall be set to '1'.

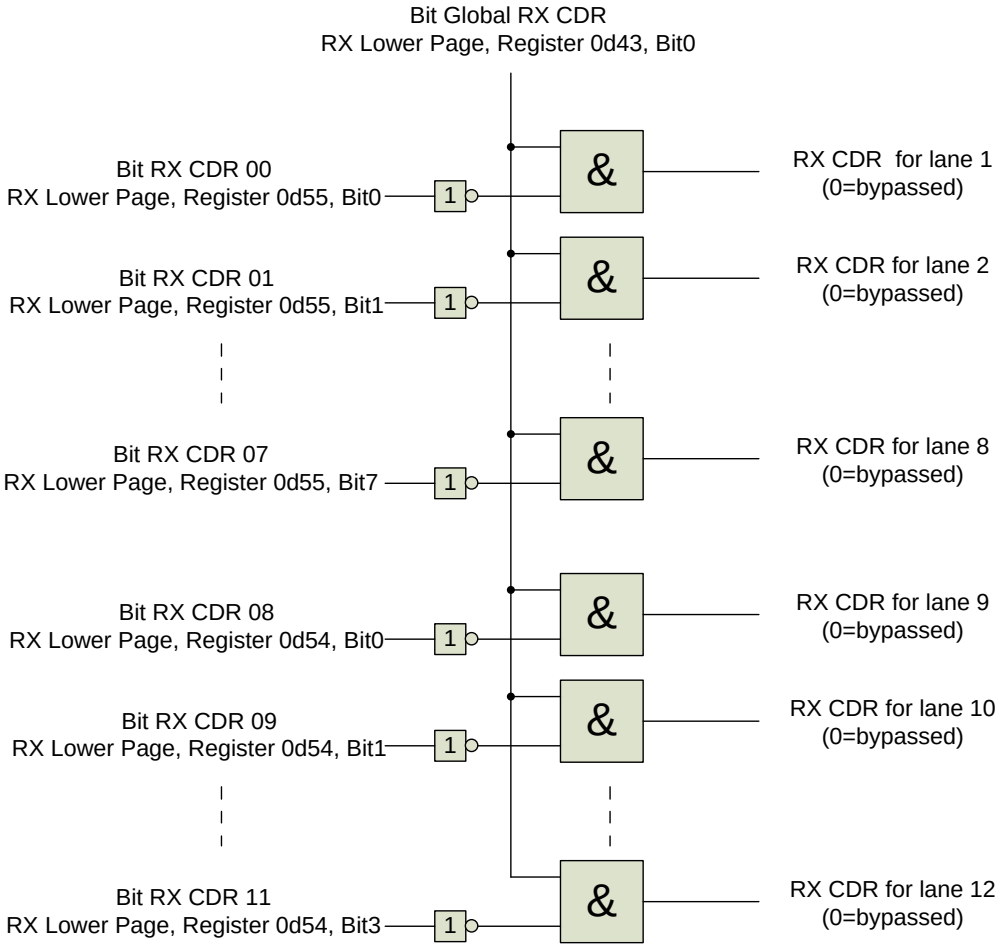


Figure 4 Rx CDR bypass

Squelch

TX Squelch

The On Board Transceiver supports Tx Squelch function. Tx Squelch functionality can be disabled channel wise via Register 56 and Register 57, present at Tx Lower Page.
Furthermore the Tx Squelch threshold level can be adjusted for all channels together at Register 76 at Tx Lower Page.

Bit7/Bit4	Bit6/Bit2	Bit5/Bit1	Bit4/Bit0	Nominal Threshold Level , no DC offset at input	Threshold Accuracy
SQHYST_DIS 0: enabled (default) 1: disabled	0	0	0	2x17 mVpp	+/- 50%
	0	0	1	2x23 mVpp	+/- 30%
	0	1	0	2x29 mVpp	+/- 24%
	0	1	1	2x35 mVpp	+/- 21%
	1	0	0	2x41 mVpp	+/- 20%
	1	0	1	2x47 mVpp	+/- 21%
	1	1	0	2x53 mVpp	+/- 22%
	1	1	1	2x60 mVpp	+/- 23%

Table 2

For default a Threshold Hysteresis is enabled, that lifts the threshold level with about 50%, when the input signal is below the threshold. However, Hysteresis can be disabled by set Bit7 respectively Bit 4 to ‘1’

Maximum Ratings

Exceeding one or more of these values may cause permanent damage.

Parameter	Conditions	Symbol	Min	Max	Units
Storage Temperature		ϑ_{St}	-20	80	°C
Powered Case Temperature Range		ϑ_C	0	70	°C
Relative Humidity	Non condensing	RH	5	85	%
Power Supply Voltage		$V_{DD}RX$, $V_{DD}TX$	-0.3	3.6	V
Voltage on Low Speed Inputs		V_{IN}	-0.3	V_{cc}+0.3	V
DC Voltage at High Speed Pins		V_D	-0.5	V_{cc}+0.5	V
Differential Input Swing max	Differential peak-to-peak amplitude max, before damage, defines not recommended operating condition and AC characteristics	V_{INmax}		2.8	V_{pp}
Static Discharge Voltage	Human body model per JEDEC JESD22-A114-B			2	kV
Air Discharge to Housing	EN61000-4-2, criterion B			15	kV
Contact Discharge to Housing	EN61000-4-2, criterion B			8	kV

Table 3

Recommended Operating Conditions

General Operating Conditions

Unless otherwise noted, module operates with factory default settings at recommended operating conditions.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Case Temperature		ϑ_C	0		70	°C
V_{DD}Tx, V_{DD}Rx Supply Voltage		V_{DDTX} and VDDRX	3.135	3.3	3.465	V
Bit Error Ratio		BER			1E-12	
Data Rate per Lane	in CDR mode	DR	25		25.8	Gbit/s
	in none CDR mode		1.25			
Transition density	in CDR mode and within 0.1µs transmission time window	t_{TD_CDR}	20			%
	in none CDR mode and and within 1µs transmission time window	t_{TD}	20			%
Data DC Balance	Electrical and Optical Input Signal within 1µs transmission time window		48		52	%

Table 4

Power Consumption

Unless otherwise noted, module operates at recommended operating conditions.
Module operates with factory default settings.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Power Consumption	Note 1	P_{Plug}		5.8	7.9	W
	Note 2			4.7	6.4	
	Note 3			2.9	4.2	
Supply Current VDDRX	Note 1	$I_{DD}RX$		0.89	1.10	A
	Note 2			0.56	0.67	
	Note 3			0.36	0.48	
Supply Current VDDTX	Note 1	$I_{DD}TX$		0.86	1.18	A
	Note 2			0.86	1.18	
	Note 3			0.51	0.74	

Table 5

Note 1: all CDRs are enabled (at RX and TX side), Receiver De-Emphasis and Receiver Output Voltage Swing as well as Transmitter Input Equalizer is set to maximum level.

Note 2: only TX CDR is enabled, Receiver De-Emphasis and Receiver Output Voltage Swing as well as Transmitter Input Equalizer are set to maximum level.

Note 3: no CDRs are enabled, De-Emphasis is not used, Receiver Output Voltage Swing is set to minimum, and Transmitter Input Equalizer is set to ‘0’

Test Points Definition

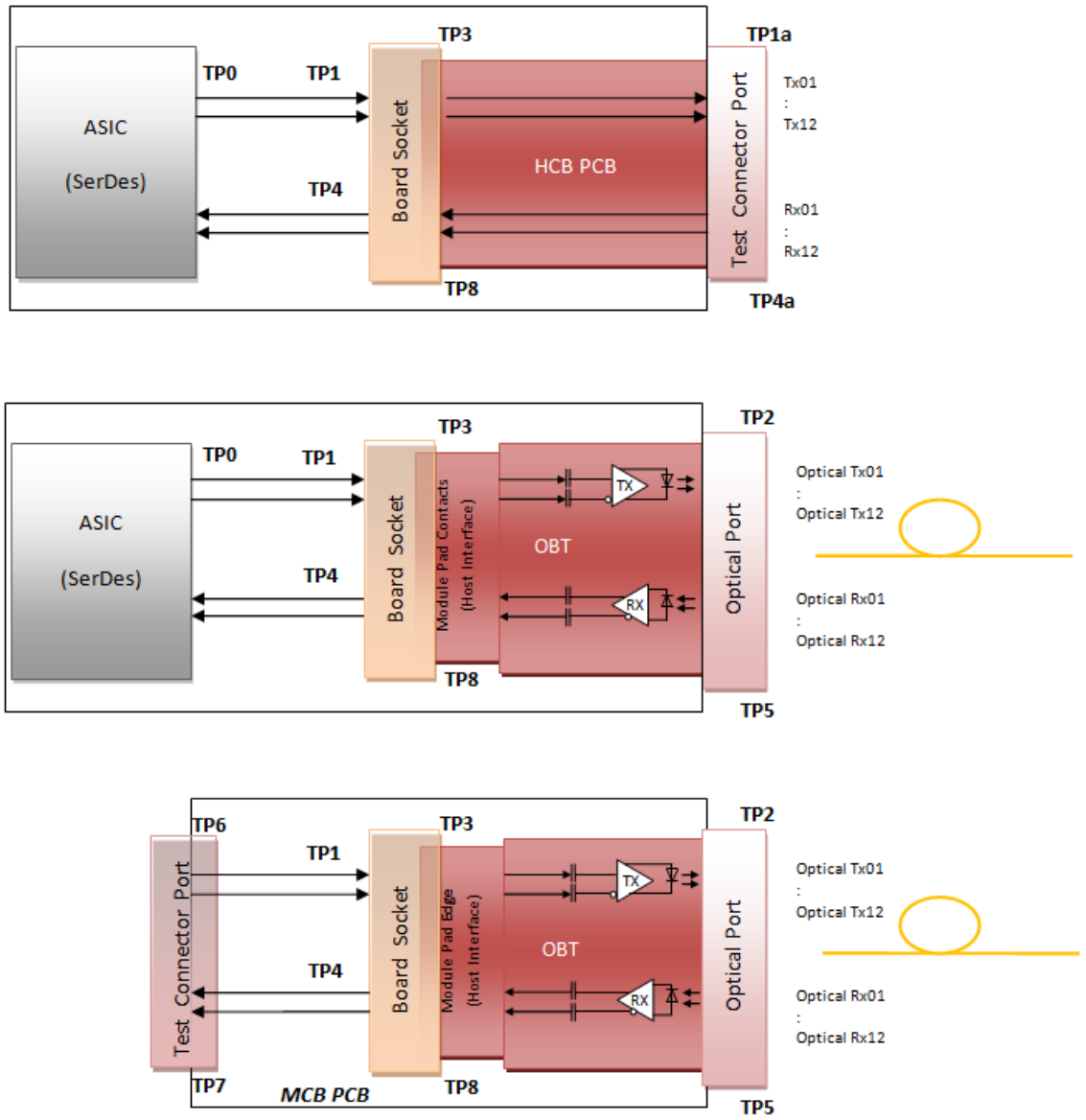


Figure 5 Test point Definitions

Module Input Characteristics

Unless otherwise noted, module operates with factory default settings at recommended operating conditions.
Referred to TP1a. Data rate is 25.78125 GBit/s.

Parameter	Conditions		Symbol	Min	Typ	Max	Units
Bit Rate with CDR			T_{Baud_CDR}	25		25.8	Gbit/s
Bit Rate without CDR			T_{Baud}	1.25		25.8	Gbit/s
Differential input voltage peak-peak swing with no equalization			$V_{DI,diff}$	2x100		2x450	mVpp
Differential Input Termination Resistance			R_{DI}	80	100	120	Ω
Data Input Coupling Capacitance	per lane;		C_C		100		nF
Differential Input Return Loss	referred to R_G = 100 Ω	f = 0.05…4 GHz	S_{DD11}			-11	dB
		f = 4…28 GHz				-6 + 9.2log(2f/28GHz)	dB
Common to Differential Conversion	referred to R_G = 100 Ω	f = 0.05…14 GHz	S_{DC11}			-22 + 14*(f/28GHz)	dB
		f = 14…28 GHz				-18+6*(f/28GHz)	
CDR Loop bandwidth	-3dB Corner		PLL_{bw}	10			MHz

Table 6

Input Equalizer

The input stage comprises a two-pole CTLE (Continuous Time Linear Equalizer).
The high frequency pole at 12GHz is programmable, the peaking of the transfer function can be adjusted from 0dB (default) up to 11dB in 16 different settings.

Tx Lower Page

Dec	Bit	MSA name	MSA description	R/W	Default Value
62	7 - 4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. High frequency pole at 12GHz Peaking Range: 0000b = 0dB . . . 1111b = 11dB.	R/W	0000b
	3 - 0	Input Equalization Tx10			0000b
63	7 - 4	Input Equalization Tx09		R/W	0000b
	3 - 0	Input Equalization Tx08			0000b
64	7 - 4	Input Equalization Tx07		R/W	0000b
	3 - 0	Input Equalization Tx06			0000b
65	7 - 4	Input Equalization Tx05		R/W	0000b
	3 - 0	Input Equalization Tx04			0000b
66	7 - 4	Input Equalization Tx03		R/W	0000b
	3 - 0	Input Equalization Tx02			0000b
67	7 - 4	Input Equalization Tx01		R/W	0000b
	3 - 0	Input Equalization Tx00			0000b

Table 7

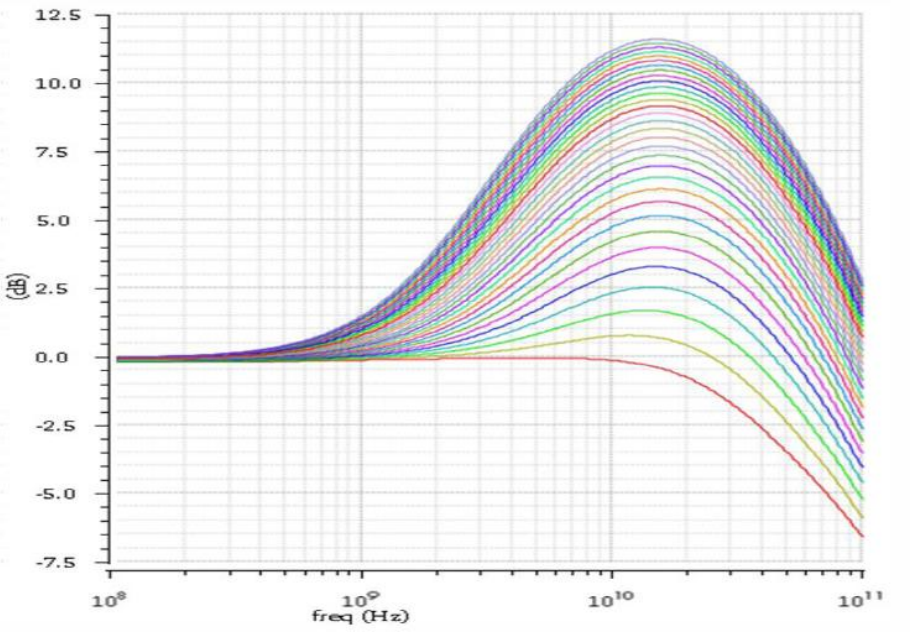


Figure 6 Frequency response of equalizer

The second pole boosts frequencies around 2GHz up, in a range from 0dB to 4dB.

TX Lower Page

Dec	Bit	MSA name	MSA description	R/W	Default Value
68	7 - 4	Input Mid Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Mid frequency pole at 2GHz Peaking Range: 0000b = 0dB . . . 1111b = 4dB.	R/W	0000b
	3 - 0	Input Mid Equalization Tx10			0000b
69	7 - 4	Input Mid Equalization Tx09		R/W	0000b
	3 - 0	Input Mid Equalization Tx08			0000b
70	7 - 4	Input Mid Equalization Tx07		R/W	0000b
	3 - 0	Input Mid Equalization Tx06			0000b
71	7 - 4	Input Mid Equalization Tx05		R/W	0000b
	3 - 0	Input Mid Equalization Tx04			0000b
72	7 - 4	Input Mid Equalization Tx03		R/W	0000b
	3 - 0	Input Mid Equalization Tx02			0000b
73	7 - 4	Input Mid Equalization Tx01		R/W	0000b
	3 - 0	Input Mid Equalization Tx00			0000b

Table 8

Optical Transmitter Characteristics

Unless otherwise noted, module operates with factory default settings at recommended operating conditions, in normal Tx Power Mode. Data rate is 25.78125 GBit/s.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Center wavelength			840		861	nm
RMS spectral width	Standard deviation of spectrum			0.5		nm
Average launch power	EOL	TxP_{AVG}	-5		3	dBm
Transmit OMA per lane	EOL	TxOMA	-3		3	dBm
Transmitter and dispersion eye closure (TDEC)					4.3	dB
Difference in launch power between lanes (OMA)					4	dB
Optical Extinction ratio		ER	3			dB
Optical return loss tolerance		ORL			12	dB
Eye Mask coordinates X1, X2, X3, Y1, Y2, Y3	Hit Ratio = $1.5x10^{-3}$ hits per sample	0.3, 0.38, 0.45, 0.35, 0.41, 0.5				UI
Average launch power of OFF transmitter					-30	dB

Table 9

Note1: Even if the TDEC < 0.9 dB, the OMA (min) exceed this value.

Receiver Optical Specification

Unless otherwise noted, module operates with factory default settings at recommended operating conditions.

Parameter	Comments	Symbol	Min	Typ	Max	Units
Center wavelength			840		861	nm
Average Input Power Damage Threshold		DT	3.4			dBm
Average receive power max, each lane	BER=1E-12, PRBS31	Rx_{avg_max}			3	dBm
Stressed Receiver Sensitivity (OMA)	Note 1	Rx_{OMA_Stress}			-4.5	dBm
Receiver Reflectance		RRf			-12	dB
LOS assert level		LOS_A	-30			dBm
LOS de-assert level		LOS_D		-12		dBm

Table 10

Note1: Stressed Receiver Sensitivity (OMA) is defined for a BER=1E-12, NEXT and FEXT aggressors on, Victim and Aggressor data rate at 25.78125 Gbit/s, Test pattern is PRBS31, Aggressor RxOMA at -2.5dBm, Victim signal with applied Jitter degradation set to J2 = 0.37UI / J9 = 0.53UI, sinusoidal 200MHz jitter added, electrical Crosstalk Amplitude = 900mV

Module Output Characteristics

Unless otherwise noted, module operates with factory default settings at recommended operating conditions.
Data rate is 25.78125 GBit/s. Data output signals are AC coupled within the OBT.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Output Coupling Capacitance	per lane	C_K		100		nF
Maximum Receicer Differential Output Voltage, pk-pk		$V_{DO\_diff\ max}$		2x240		mVpp
Receicer Differential Output Voltage Stepsize, pk-pk	Nominal Differential peak peak high-speed data output voltage step size 100 Ω differential Termination. 8 levels	$V_{DO\_diff\ Stepsize\_LSB}$		2x30		mVpp
Emphasis Level		V_{DO_De}	*See page 19,* Receiver Voltage Output Swing and Emphasis Setting			
De-Emphasis Delay 25G		t_{DE_25G}		33		ps
Common mode noise. rms					17.5	mV
Differential Termination Missmatch	at 1 MHz				10	%
Differential Output Return Loss	referred to R_G = 100 Ω; f = 0.05…4 GHz	S_{DD22}			-11	dB
	referred to R_G = 100 Ω; f = 4…28 GHz				-6 + 9.2log(2f/28GHz)	
Common Mode to Differential Conversion Return Loss	referred to R_G = 100 Ω; f = 0.05…14 GHz	S_{DC22}			-25 + 20 * (f/28GHz)	dB
	referred to R_G = 100 Ω; f = 14…28 GHz				-18 + 6*(f/28GHz)	
Common Mode Return Loss (SCC22)	from 250 MHz to 30 GHz			-2		dB
Transition Time: 20/80%			9.5			ps
Vertical Eye Clousure (VEC)					5.5	dB
Eye width at 10^{-15} probability (EW15)	Note 1	EW15	0.57			UI
Eye heigth at 10^{-15} probability (EH15)	Note 2	EH15	228			mV

Table 11

Note1: Module setting: Rx CDR on, Rx Amplitude maximum, De-emphasis =8
Note2: Module setting: Rx CDR on, Rx Amplitude maximum, De-emphasis =0, Scope CTLE = 1dB setting, de-embedded setup loss

Receiver Voltage Output Swing and Emphasis Setting

The CML data outputs supports programmable emphasis and output amplitude. Nominal differential output peak-peak value (V_{DO_diff}) without emphasis has a range from 2x30mV to 2x240mV in eight equivalent steps.

Output Amplitude can be controlled via Register 62 to 67, De-Emphasis via Register 68 to 73. Both registers are located at Lower Receiver Memory Page.

A Register byte is used to control two electrical channels, as shown in example below.

Dec	Bit	Description
62	7 - 5	Output Amplitude RX11 A writing 111b calls for full-scale signal amplitude. A writing 000b calls for minimum signal amplitude.
	4	Not used
	3 - 1	Output Amplitude RX10 A writing 111xb calls for full-scale signal amplitude. A writing 000xb calls for minimum signal amplitude.
	0	Not used

You can set the Amplitude or De-Emphasis Registers in a range from 0 to 15.
However, since Bit 0 respectively Bit 4 is not used, you have effectively 8 different levels available.

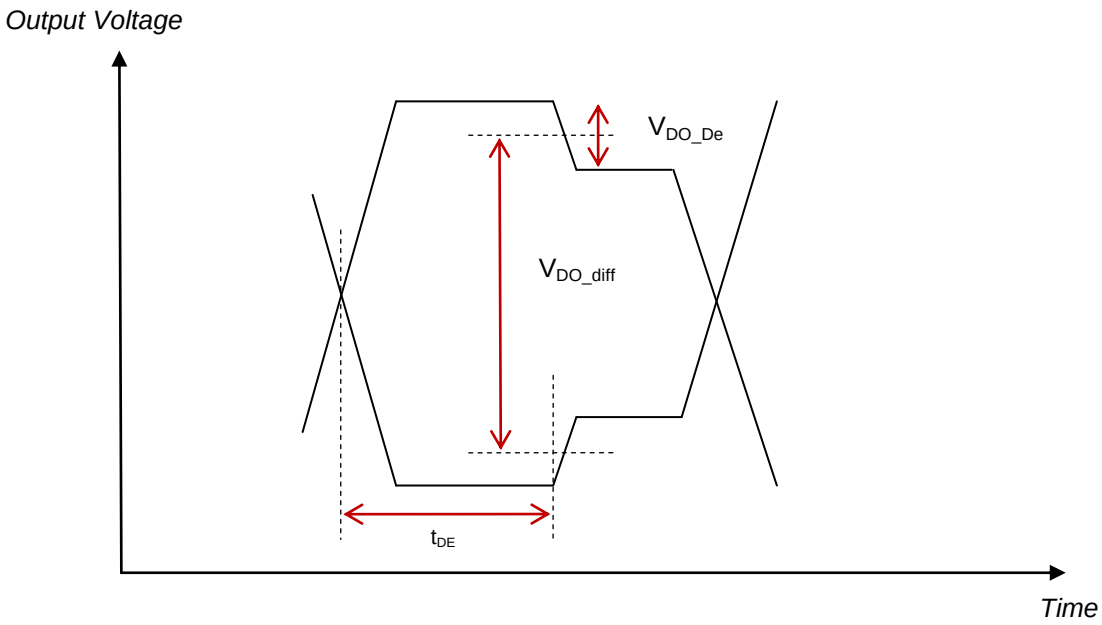


Figure 7 Receiver Voltage Output Swing and Emphasis Setting

The relationship V_{DO_Diff} can be calculate with

$$V_{DO\_Diff} = 2 \times 30mV \times (<\text{Output Amplitude RX}>_{Reg} + 1)$$

<Output Amplitude RX >$_{Reg}$ represents value of the 3 register bits for Emphasis level, Bit 7-5 or Bit 3-1.

The relationship V_{DO_De} can be calculate with

$$V_{DO\_De} = V_{DO\_Diff} \times (<\text{Output De-emphasis RX}>_{Reg}) \times 4.8\%$$

Output De-emphasis RX09 represents value of the 3 register bits for Emphasis level, Bit 7-5 or Bit 3-1.

Low Speed I/O Characteristics

Unless otherwise noted, module operates with factory default settings at recommended operating conditions.
Output pin INT_L
Input pins RST_L, Address Pins A0, A1, A2, A3

Parameter	Conditions	Symbol	Min	Typ	Max	Units
DC-Characteristics						
Input Voltage Low	|Iin| <= 370µA for 0V< Vin < Vcc	V_{IL}	-0.3		0.8	V
Input Voltage High		V_{IH}	2.4		Vcc+0,3	V
Output Voltage Low	I_{OL} = 2mA	V_{OL}	0		0.4	V
Output Voltage High		V_{OH}	Vcc-0.3		Vcc+0.3	V

Table 12

Serial Management Interface (SDA / SCL)

Recommended Operating Conditions

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Voltage Low		V_{IL}	-0.3		0.4	V
Input Voltage High		V_{IH}	2.4		Vcc+0.3	V
Pull-Up Resistance	Absolute range	R_{PU}	1.1		13	kΩ
	Recommended range depends on total capacitive and current load of the bus	R_{PU}	$\frac{3.465V - 0.3V}{3mA - I_{L\,max}}$		$\frac{3.135V - 2.8V}{I_{QH\,max}}$	Ω
					$\frac{420ns}{\ln 9 \cdot C_{B\,max}}$	Ω
Total Bus Load	R_{PU} ≤ 3 kΩ [1])	C_B			100	pF
	R_{PU} ≤ 1.6 kΩ [1])	C_B			200	pF
Timing						
Clock Frequency		f_{SCL}	0		400	kHz
Clock Pulse Width Low	Width for V_I ≤ 0.4 V	t_{LSCL}	1.3			µs
Clock Pulse Width High	Width for V_I ≥ 2.1 V	t_{HSCL}	600			ns
START Set Up Time		$t_{s,STA}$	600			ns
START Hold Time		$t_{h,STA}$	600			ns
STOP Set Up Time		$t_{s,STO}$	600			ns
Data Setup Time		t_s	250			ns
Data Hold Time		t_h	0			ns
Bus Free Time	Time between STOP and START or between ACK and RESTART	t_{BUF}	20			µs
Rise Time	SDA and SCL, V_{ILmax} to V_{IHmin}	t_R			300	ns
	SDA and SCL, equivalent 10%-90% value				420	ns
Fall Time	SDA and SCL, V_{IHmin} to V_{ILmax}	t_F			300	ns
	SDA and SCL, equivalent 10%-90% value				420	ns

Table 13

1) Definition due to OBT specification. However, with these pull-up resistor values the rise time definitions of the OBT specification will not be met. With these combinations the rise time goes up from 300 ns to 471 ns (3 kΩ, 100 pF) and to 457 ns (1.6 kΩ, 200 pF) respectively.

Characteristics

Characteristics are valid under recommended operating conditions.

Parameter	Conditions		Symbol	Min	Typ	Max	Units
Static Characteristics							
Output Voltage Low	I_{OL} = 3 mA		V_{OL}	0		0.3	V
Output Current High	Vo = -0.3 V…3.6 V		I_{OH}	-10		10	µA
Output Voltage High			V_{OH}	2.8		3.6	V
Dynamic Characteristics							
Input Capacitance			C_I			14	pF
Data Setup Time			t_s	100			ns
Data Hold Time			t_h	0			ns
Output Rise Time	SDA and SCL RPU = 1.1 kΩ ± 2%, C_L = 170 pF	V_{ILmax} to V_{IHmin}	t_R			300	ns
		10% to 90%				420	ns
Output Fall Time	SDA and SCL RPU = 1.1 kΩ ± 2%, C_L = 170 pF	V_{IHmin} to V_{ILmax}	t_F			300	ns
		10% to 90%				420	ns
Clock Stretching Time			$t_{Clkhold}$			500	µs
Write Cycle Endurance	ϑC ≤ 70°C					50000	Cycles

Table 14

Timing Characteristics

Characteristics are valid under recommended operating conditions.

Parameter	Conditions/Remark	Symbol	Min	Typ	Max	Units
Initialization Time	Time from power up or reset to clearing of Data Not Ready Flag (page A0, byte 2, bit 0) and INT_L assertion	t_{data}			2	s
Interrupt Assert Time	Time from condition occurrence to setting of INT Bit (page A0, byte 2, bit 1) and reporting on at interrupt status output INT_L/RST_L	t_{INTon}			100	ms
Rx-Loss Assert Time	Time from Rx-Loss state to setting of Rx-Loss Bit and INT_L assertion	$t_{LOS,on}$			100	ms
Flag Assert Time	Time from flag condition occurrence to setting of related Flag Bit and INT_L Assertion	$t_{Flag,on}$			100	ms
Interrupt De-Assert Time	Time from read of associated Flag Bit to clear of INT Bit (0xA0, byte 2, bit 1)	t_{INToff}			500	µs

Table 15

Management Interface Device Addresses

A0, A1, A2, A3 Pins

A0,A1,A2 and A3 represents the address pins for the 2-wire interface.

I2C Device	I2C Address	
	HEX	Binary
Transmitter	0xA0-0xBE	1 0 1 A_3 A_2 A_1 A_0 x
Receiver	0x80-0x9E	1 0 0 A_3 A_2 A_1 A_0 x

Table 16

x=Read/Write -Bit

I2C uses A0,A1,A2 only.
In standard I2C operation, A3 should be set to logical low.

By setting A3 to logical high interface does not used the standard I2C addressing scheme but allows a system to address more than 8 OBT devices on same serial bus, when required.

Memory Organization

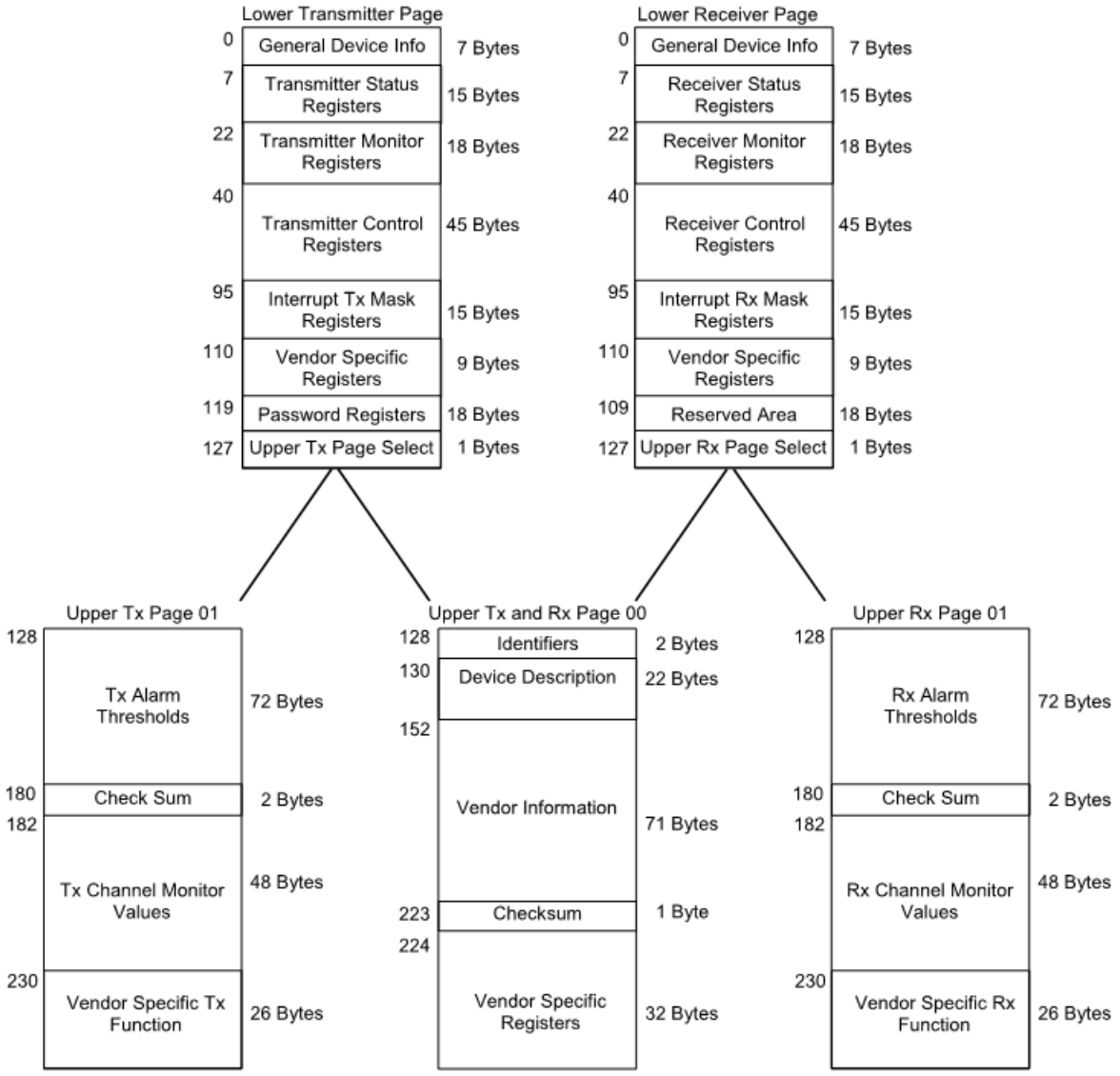


Figure 8 Memory Map

Upper Page 2 not shown in Memory Map above, but supported by OBT.

Page Overviews

'x' indicates a variable value.
Suffix 'b' for binary value eg. 01b. Suffix 'h' for hexadecimal value eg. FFh.

Lower Transmitter Memory Page

Dec	Bit	MSA name	MSA description	R/W	Default Value
0	all	Reserved	Coded 00h (unspecified)	R	00h
1	all	Reserved: Extended Status	00h	R	00h
2	7 - 6	Reserved	00b	R	00b
	5 - 4	Tx and/or Rx Upper Page 02 Presence	00b = no optional Upper Page 02 supported 10b = Upper Page 02 supported, Tx address 01b = Upper Page 02 supported, Rx address 11b = Upper Page 02 supported, accessible through either Tx address or Rx address	R	11b
	3	Rx Device Address Presence	0 = Rx Device Address fields are present. 1 = Rx Device Address fields are not present	R	0b
	2	Flat/Paging Memory Presence	0 = Paging is present. 1 = Upper Page 00h only, no other Tx Upper pages	R	0b
	1	Int_L Status	coded 1 for asserted Int_L. Clears to 0 when all flags including LOS and Fault are cleared	R	xb
	0	Data_Not_Ready	Indicates transceiver has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low	R	xb
3	all	Version Control	undefined	R	0b
4-5	all	Reserved		R	00h
6	7	LOS Tx Status Summary	Coded 1 when a LOS Tx flag (bytes 7-8) is asserted for any channel, else 0. Clears when LOS flags are cleared.	R	xb
	6	Reserved	Coded 0b. Reserved for Rx LOS Status Summary in Rx Lower Page	R	0b
	5	Fault Tx Status Summary	Coded 1 when a Fault Tx flag (bytes 9-10) is asserted for any channel, else 0. Clears when Fault flags are cleared	R	xb
	4	Bias Tx Status Summary	Coded 1 when a Tx Bias Hi-Lo Alarm (bytes 11-13) is asserted, else 0. Clears when alarm is cleared.	R	0b
	3	CDR LOL Tx Status Summary	Coded 1 when a TX CDR LOL (bytes 15-16) is asserted., else 0. Clears when alarm is cleared.	R	xb
	2	Reserved	Coded 0b. Reserved for Rx Optical Power Hi-Lo Alarm in Rx Lower Page	R	0b
	1	Module Tx Status Summary	Coded 1 when any flag is set on Bytes 17-21. Including: Tx Temperature Alarms Intitialization Complete flag Tx Voltage alarms reserved Module Tx monitor alarm Coded 0 when all regarding flags are cleared.	R	xb
	0	Reserved	Reserved for other Module Monitor alarm	R	0b
7	7 - 4	Reserved	Loss of Signal Tx Channel: coded 1 when asserted, Latched, Clears on Read.	R	0000b
	3 - 0	L-LOS Tx11 - Tx08		R	xxxxb
8	all	L-LOS Tx07 - Tx00		R	xxh

Dec	Bit	MSA name	MSA description	R/W	Default Value
9	7 - 4	Reserved	Fault Tx Channel: Coded 1 when asserted, Latched, Clears on Read.	R	0000b
	3 - 0	L-Fault Tx11 - Tx08		R	xxxxb
10	all	L-Fault Tx07 - Tx00		R	xxh
11	all	L-Bias Hi-Lo Alarm Tx11 - Tx08	not supported	R	00h
12	all	L-Bias Hi-Lo Alarm Tx07 - Tx04		R	00h
13	all	L-Bias Hi-Lo Alarm Tx03 - Tx00		R	00h
14	All	Reserved		R	00h
15	7 - 4	Reserved		R	0000b
	3 - 0	LOL Tx11 - Tx08	Loss of Lock, Tx CDR: Coded 1 when asserted (i.e., when CDR is enabled and not locked to data stream), 0 when (CDR is enabled AND locked) OR (CDR is bypassed). Unlatched.	R	xxxxb
16	7 - 0	LOL Tx07 - Tx00		R	xxh
17	7	L-Temp High Alarm - Tx	High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	xb
	6	L-Temp Low Alarm - Tx	Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	xb
	5 .. 1	Reserved		R	00000b
	1	Initialization Complete flag	Asserted after initialization and /or reset has completed. Clear to zero when read		xb
18	7	L-Vcc3.3 High Alarm - Tx	High Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	xb
	6	L-Vcc3.3 Low Alarm - Tx	Low Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	xb
	5 .. 4	Reserved		R	00b
	3	L-VccHI Low Alarm - Tx	Low Internal VccHI Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	0b
	2	L-VccHILow Alarm - Tx	Low Internal VccHI Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	0b
	1 .. 0	Reserved		R	00b
19	All	Reserved	Vendor Specific	R	00h
20	all	Reserved	Vendor Specific	R	00h
21	all	Reserved	Vendor Specific	R	xxh
22	7 - 0	1st Tx Temp Monitor MSB	1st Internal Temperature Monitor for Tx MSB: Integer part coded in signed 2's complement. Tolerance is ± 3°C.	R	xxh
23	7 - 0	1st Tx Temp Monitor LSB	1st Internal Temperature Monitor for Tx LSB: Fractional part in units of 1°/256 coded in binary.	R	xxh
24	all	2nd Tx Temp Monitor MSB	not supported	R	00h
25	all	2nd Tx Temp Monitor LSB	not supported	R	00h
26	7 - 0	Tx Vcc3.3 Monitor MSB	Internal Vcc3.3 Monitor for Tx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.10V.	R	xxh
27	7 - 0	Tx Vcc3.3 Monitor LSB		R	xxh
28	7 - 0	Tx VccHI Monitor MSB	Internal VccHI Monitor for Tx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.10V.	R	xxh
29	7 - 0	Tx VccHI Monitor LSB		R	xxh
30-37	all	Reserved	Reserved - Module Monitors	R	00h
38	all	Elapsed Operating Time	not supported	R	00h
39				R	00h
40	all	Tx Module Application select	Not supported	R	00h

Dec	Bit	MSA name	MSA description	R/W	Default Value
41	7 - 5	Reserved	Reserved - Rate Select	R	000b
	4 - 0	Tx Rate Select	Tx Rate Select / optimization bit-map Bit 4: EDR Bit 3:FDR Bit 2: QDR Bit 1: DDR Bit 0:SDR Examples: 00111: Configured for QDR / DDR / SDR operation 01000: Configured for FDR operation 10000: Configured for EDR operation 00000: no info provided	R	11111b
42	7 - 1	Reserved		R	0000000b
	0	High-Power Mode	0: Device or cable may not draw more than 6 Watts of power. 1: Device or cable may draw more than 6.0 W, up to limit denoted in Upper Page 00, Byte 148(94h)	R	1b
43	7 - 1	Reserved		R	0000000b
	0	Global TX CDR	0: all CDR off 1: TX CDR follows individual setting at Register 0x54 and 0x55. (all TX CDR will be enabled at once, as long as Register 0x54 and 0x55 kept in default state)	R/W	xb
44-50	all	Reserved	Reserved - Module Control	R	00h
51	7 - 1	Reserved		R/W	0000000b
	0	Reset	Reset: Writing 1 return all registers (non-volatile RW, if present in vendor-specific area) to factory default values. Reads 0 after operation.		xb
52	7 - 4	Reserved	Not supported	R/W	0000b
	3 - 0	Channel Disable Tx11 - Tx08			0000b
53	7 - 0	Channel Disable Tx07 - Tx00		R/W	00h
54	7 - 4	Reserved	1: CDR will be individual bypassed	R/W	0000b
	3 - 0	TX CDR 11 - TX CDR 08		R/W	xxxxb
55	7 - 0	TX CDR 07 - TX CDR 00		R/W	xxh
56	7 - 4	Reserved	Tx Squelch Disable: Writing 1 disables squelch for the channel (default value) 0 enables squelch function.	R/W	0000b
	3 - 0	Squelch Disable Tx11 - Tx08		R/W	xxxxb
57	7 - 0	Squelch Disable Tx07 - Tx00		R/W	xxh
58	7 - 4	Reserved	Tx Channel input polarity flip: Writing 1 inverts the polarity of outputs relative to the inputs. Default is 0 (No polarity flip)	R/W	0000b
	3 - 0	Polarity flip Tx11 - Tx08			xxxxb
59	7 - 0	Polarity flip Tx07 - Tx00		R/W	xxh
60	7 - 4	Reserved	not supported	R	0000b
	3 - 0	Margin Select Tx11 - Tx08		R	0000b
61	7 - 0	Margin Select Tx07 - Tx00		R	00h
62	7 - 4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. High frequency pole at 12GHz Peaking Range: **0000b = 0dB (default)** . . . 1111b = ~11dB.	R/W	xxxxb
	3 - 0	Input Equalization Tx10			xxxxb
63	7 - 4	Input Equalization Tx09		R/W	xxxxb
	3 - 0	Input Equalization Tx08			xxxxb
64	7 - 4	Input Equalization Tx07		R/W	xxxxb
	3 - 0	Input Equalization Tx06			xxxxb
65	7 - 4	Input Equalization Tx05		R/W	xxxxb
	3 - 0	Input Equalization Tx04			xxxxb
66	7 - 4	Input Equalization Tx03		R/W	xxxxb
	3 - 0	Input Equalization Tx02			xxxxb

Dec	Bit	MSA name	MSA description	R/W	Default Value
67	7 - 4	Input Equalization Tx01		R/W	xxxxb
	3 - 0	Input Equalization Tx00			xxxxb
68	7 - 4	Input Mid Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. High frequency pole at 2GHz Peaking Range: **0000b = 0dB (default)** .1111b = ~4dB.	R/W	xxxxb
	3 - 0	Input Mid Equalization Tx10			xxxxb
69	7 - 4	Input Mid Equalization Tx09		R/W	xxxxb
	3 - 0	Input Mid Equalization Tx08			xxxxb
70	7 - 4	Input Mid Equalization Tx07		R/W	xxxxb
	3 - 0	Input Mid Equalization Tx06			xxxxb
71	7 - 4	Input Mid Equalization Tx05	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. High frequency pole at 2GHz Peaking Range: **0000b = 0dB (default)** .1111b = ~4dB.	R/W	xxxxb
	3 - 0	Input Mid Equalization Tx04			xxxxb
72	7 - 4	Input Mid Equalization Tx03		R/W	xxxxb
	3 - 0	Input Mid Equalization Tx02			xxxxb
73	7 - 4	Input Mid Equalization Tx01		R/W	xxxxb
	3 - 0	Input Mid Equalization Tx00			xxxxb
74	7 - 4	Reserved	**SQHYST_DIS** Squelch Hysteresis enabled: 0b (default) Squelch Hysteresis disabled: 1b	R/W	xxxxb
	3 - 0	SQHYST_DIS Tx11 - Tx08			xxxxb
75	7 - 0	SQHYST_DIS Tx07 - Tx00		R/W	xxh
76	7-3	Tx Input Squelch Hysteresis Threshold	Reserved	R/W	xxxxxb
	2 - 0		TX Input Squelch Threshold level Bit 0-2: 000b = 2x17mVpp 001b = 2x23mVpp 010b = 2x29mVpp 011b = 2x35mVpp (default) 100b = 2x41mVpp 101b = 2x47mVpp 110b = 2x53mVpp 111b = 2x60mVpp	R/W	xxxb
77-94	all	Reserved	Reserved - Per-Channel Control	R/W	xxh
95	7 - 4	Reserved	Mask Tx LOS Flag: Writing 1 prevents Int_L on Tx LOS. Default = 0	R/W	0000b
	3 - 0	Mask LOS Flag Tx11 - Tx08			xxxxb
96	7 - 0	Mask LOS Flag Tx07 - Tx00		R/W	xxh
97	7 - 4	Reserved	Mask Tx Fault Flag: Writing 1 prevents Int_L on Tx Fault. Default = 0	R/W	0000b
	3 - 0	Mask Tx Fault Flag Tx11 - Tx08			xxxxb
98	7 - 0	Mask Tx Fault Flag Tx07 - Tx00		R/W	xxh
99	7 - 0	Mask Bias Hi-Lo Alarm Tx11 - Tx08	not supported	R/W	xxh
100	7 - 0	Mask Bias Hi-Lo Alarm Tx07 - Tx04		R/W	xxh
101	7 - 0	Mask Bias Hi-Lo Alarm Tx03 - Tx00		R/W	xxh
102	all	Reserved	Reserved	R/W	0h
103	7 – 4	Reserved	Mask Tx LOL Flag: Writing 1 prevents Int_L on Tx Loss of Lock on Tx CDR. Default = 0, mask is required if corresponding optional alarm is implemented.	R/W	0000b
	3 - 0	Mask LOL Flag Tx11 - Tx08		R/W	xxxxb
104	7 - 0	Mask LOL Flag Tx17 - Tx00		R/W	xxh
105	7	Mask Temp High Alarm - Tx	Mask High Internal Temperature Alarm: Writing 1 prevents Int_L on High Tx Internal temperature. Default = 0	R/W	xb
	6	Mask Temp Low Alarm - Tx	Mask Low Internal Temperature Alarm: Writing 1 prevents Int_L on Low Tx internal temperature. Default = 0	R/W	xb

	5 - 0	Reserved	Reserved	R/W	000000b
Dec	**Bit**	**MSA name**	**MSA description**	**R/W**	**Default Value**
106	7	Mask Vcc3.3-Tx High Alarm	Mask High Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on High Vcc3.3-Tx Voltage alarm. Default = 0	R/W	xb
	6	Mask Vcc3.3- Low Alarm	Mask Low Internal 3.3 Vcc Alarm: Writing 1 prevents nt_L on Low Vcc3.3-Tx Voltage alarm. Default = 0	R/W	xb
	5 - 4	Reserved	Reserved	R/W	00b
	3	Mask Vcc12-Tx High Alarm	not supported	R/W	0b
	2	Mask Vcc12-Tx Low Alarm	not supported	R/W	0b
	1 - 0	Reserved	not supported	R/W	0b
107-115	all	Reserved		R/W	xxb
116	all	Vendor Specific	Vendor Specific Read - Write Registers for Tx	R/W	xxb
	7 - 4	Reserved		R/W	0000b
117	3 - 0	Output Disable Tx11 - Tx08	Tx Output Disable: Writing 1 disables just the output for the channel. Default is 0 (Output Enabled or controlled by Squelch function).	R/W	xxxxb
118	7 - 0	Output Disable Tx07 - Tx00	Tx Output Disable: Writing 1 disables just the output for the channel. Default is 0 (Output Enabled or controlled by Squelch function).	R/W	xxh
119	all	Reserved Password Change Entry Area	Password Change Entry Area for Tx register space	R/W	00b
120	all			R/W	xxh
121	all			R/W	xxh
122	all			R/W	xxh
123	all	Password Entry Area	Password Entry Area for Tx register space	R/W	xxh
124	all			W	xxh
125	all			W	xxh
126	all			W	xxh
127	all	Page Select	Selects Upper Page - Required if paging is used on upper page(s). Not required if paging is not used. Writing 00h selects Tx & Rx Upper Page 00h Writing 01h selects Tx Upper Page 01h, etc.	R/W	xxh

Lower Receiver Memory Page

Dec	Bit	MSA name	MSA description	R/W	Default Value
0	All	Reserved	Coded 00h (unspecified)	R	00h
1	All	Reserved: Extended Status	00h	R	00h
2	7 - 4	Reserved		R	0000b
	3	Reserved	used in Tx Lower Page to indicate presence of Rx	R	0b
	2	Flat/Paging Memory Presence	0 = Paging is present. 1 = Upper Page 00h only, no other Rx Upper pages	R	0b
	1	Int_L Status	Coded 1 for asserted Int_L. Clears to 0 when all flags are cleared	R	xb
	0	Data_Not_Ready	are cleared.	R	xb
3	All	Version Control	undefined	R	0b
4	All	Reserved		R	00h
5	All	Reserved		R	00h
6	7	Reserved	Coded 0b. Reserved for Rx status info	R	0b
	6	LOS Rx Status Summary	Coded 1 when a LOS Rx flag (bytes 7-8) is asserted for any channel, else 0. Clears when Fault flags are cleared.	R	xb
	5 -4	Reserved	Coded 000b. Reserved for Rx status info	R	000b
	3	RX LOL Status Summary	Coded 1 when a RX CDR LOL (bytes 12-13) is asserted., else 0. Clears when alarm is cleared.	R	xb
	2	Power Rx Status Summary	not supported	R	0b
	1	Module Rx Status Summary	Coded 1 when any Rx Temperature or Voltage alarm (bytes 17-18) or reserved Module Rx monitor alarm (reserved in bytes 19-21) is asserted, else 0. Clears when Rx alarm is cleared.	R	xb
	0	Reserved	Reserved for other Module Monitor alarm	R	0b
7	7 - 4	Reserved	Loss of Signal Rx Channel: coded 1 when asserted, Latched, Clears on Read.	R	0000b
	3 - 0	L-LOS Rx11 - Rx08		R	xxxxb
8	all	L-LOS Rx07 - Rx00		R	xxh
9	7 - 4	Reserved	Fault Rx Channel: Coded 1 when asserted, Latched, Clears on Read.	R	0000b
	3 - 0	L-Fault Rx11 - Rx08		R	xxxxb
10	all	L-Fault Rx07 - Rx00		R	xxh
11	all	Reserved		R	00h
12	7 - 4	reserved	Loss of Lock, Rx CDR: Coded 1 when asserted (i.e., when CDR is enabled and not locked to data stream), 0 when (CDR is enabled AND locked) OR (CDR is bypassed). Unlatched.	R	xxxxb
	3 - 0	LOL Rx11 - Rx08			xxxxb
13	all	LOL Rx07 - Rx00		R	xxh
14	all	L-Power Hi-Lo Alarm Rx11 - Rx08	not supported	R	00h
15	all	L-Power Hi-Lo Alarm Rx07 - Rx04		R	00h
16	all	L-Power Hi-Lo Alarm Rx03 - Rx00		R	00h
17	7	L-Temp High Alarm - Rx	not supported	R	xb
	6	L-Temp Low Alarm -Rx	not supported	R	xb
	5 .. 0	Reserved		R	000000b

Dec	Bit	MSA name	MSA description	R/W	Default Value
18	7	L-Vcc3.3 High Alarm - Rx	High Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	xb
	6	L-Vcc3.3 Low Alarm - Rx	Low Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	R	xb
	5 .. 4	Reserved		R	00b
	3	L-Vcc12 High Alarm - Rx	not supported	R	0b
	2	L-Vcc12 Low Alarm - Rx	not supported	R	0b
	1 .. 0	Reserved		R	00b
19	All	Reserved	Vendor Specific	R	00h
20	All	Reserved	Vendor Specific	R	0000b
21	All	Reserved	Vendor Specific	R	xxh
22	All	1st Rx Temp Monitor MSB	not supported	R	00h
23	All	1st Rx Temp Monitor LSB	not supported	R	00h
24	All	2nd Rx Temp Monitor MSB	not supported	R	00h
25	All	2nd Rx Temp Monitor LSB	not supported	R	00h
26	All	Rx Vcc3.3 Monitor MSB	Internal Vcc3.3 Monitor for Rx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.10V.	R	xxh
27	All	Rx Vcc3.3 Monitor LSB		R	xxh
28	All	Rx Vcc12 Monitor MSB	not supported	R	00h
29	All	Rx Vcc12 Monitor LSB		R	00h
30 - 37	All	Reserved	Reserved - Module Monitors	R	00h
38	All	Elapsed Operating Time	not supported	R	00h
39				R	00h
40	All	Rx Module Application select	Format to be determined as other applications besides InfiniBand arise	R	00h
41	7 - 5	Reserved	Reserved - Rate Select	R/W	000b
	4 - 0	Rx Rate Select	Rx Rate Select / optimization bit-map Bit 4: EDR Bit 3:FDR Bit 2: QDR Bit 1: DDR Bit 0:SDR Examples: 00111: Configured for QDR / DDR / SDR operation 01000: Configured for FDR operation 10000: Configured for EDR operation 00000: no info provided	R/W	xxxxxb
42	All	Reserved	Used in Tx Lower Page to manage devices with >6.0 Watt power utilization	R	00h
43	7 - 1	Reserved		R	ro
	0	Global RX CDR	0: all CDR off 1: RX CDR follows individual setting at Register 0x54 and 0x55. (all RX CDR will be enabled at once, as long as Register 0x54 and 0x55 kept in default state)	R/W	xb
44 - 50	All	Reserved	Reserved - Module Control	R	00h
51	7 - 1	Reserved		R/W	0000000b
	0	Reset - RX	Reset: Writing 1 return all registers (non-volatile RW, if present in vendor-specific area) to factory default values. Reads 0 after operation.		xb
52	7 - 4	Reserved	Rx Channel Disable: Writing 1 disables the whole channel, Default is 0.	R/W	0000b
	3 - 0	Channel Disable Rx11 - Rx08			xxxxb
53	7 - 0	Channel DisableRx07 - Rx00		R/W	xxh

Dec	Bit	MSA name	MSA description	R/W	Default Value
54	7 - 4	Reserved	1: CDR will be individual bypassed 1: CDR will be individual bypassed	R/W	0000b
	3 - 0	RX CDR 11 - RX CDR 08			xxxxb
55	All	RX CDR 07 - RX CDR 00		R/W	xxh
56	7 - 4	Reserved	Rx Squelch Disable: Writing 1 disables squelch for the channel (default value) 0 enables squelch function.	R/W	0000b
	3 - 0	Squelch Disable Rx11 - Rx08		R/W	xxxxb
57	7 - 0	Squelch Disable Rx07 - Rx00		R/W	xxh
58	7 - 4	Reserved	Rx Channel polarity flip: Writing 1 inverts the polarity of outputs relative to the inputs. Default is 0 (No polarity flip)	R/W	0000b
	3 - 0	Polarity flip Rx11 - Rx08			xxxxb
59	7 - 0	Polarity flip Rx07 - Rx00		R/W	xxh
60	7 - 4	Reserved	not supported	R	0000b
	3 - 0	Margin Select Rx11 - Rx08		R	0000b
61	7 - 0	Margin Select Rx07 - Rx00		R	00h
62	7 - 5	Output Amplitude RX11	Rx Output Amplitude Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Bit 4 and Bit 0 are don't care. Writing 111xb calls for full-scale signal amplitude. Writing 000xb calls for minimum signal amplitude. Writing intermediate code values calls for intermediate levels of signal amplitude.	R/W	xxxb
	4	Not used			0b
	3 - 1	Output Amplitude RX10			xxxb
	0	Not used			0b
63	7 - 5	Output Amplitude RX09		R/W	xxxb
	4	Not used			0b
	3 - 1	Output Amplitude RX08			xxxb
	0	Not used			0b
64	7 - 5	Output Amplitude RX07		R/W	xxxb
	4	Not used			0b
	3 - 1	Output Amplitude RX06			xxxb
	0	Not used			0b
65	7 - 5	Output Amplitude RX05		R/W	xxxb
	4	Not used			0b
	3 - 1	Output Amplitude RX04			xxxb
	0	Not used			0b
66	7 - 5	Output Amplitude RX03		R/W	xxxb
	4	Not used			0b
	3 - 1	Output Amplitude RX02			xxxb
	0	Not used			0b
67	7 - 5	Output Amplitude RX01		R/W	xxxb
	4	Not used			0b
	3 - 1	Output Amplitude RX00			xxxb
	0	Not used			0b
68	7 - 5	Output De-emphasis RX11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Bit 4 and Bit 0 are don't care. Writing 111xb calls for full-scale De-emphasis. Writing 000xb calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	R/W	xxxb
	4	Not used			0b
	3 - 1	Output De-emphasis RX10			xxxb
	0	Not used			0b
69	7 - 5	Output De-emphasis RX09		R/W	xxxb
	4	Not used			0b
	3 - 1	Output De-emphasis RX08			xxxb
	0	Not used			0b
70	7 - 5	Output De-emphasis RX07		R/W	xxxb

Dec	Bit	MSA name	MSA description	R/W	Default Value
	4	Not used	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Bit 4 and Bit 0 are don't care. Writing 111xb calls for full-scale De-emphasis. Writing 000xb calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.		0b
	3 - 1	Output De-emphasis RX06			xxxb
	0	Not used			0b
71	7 - 5	Output De-emphasis RX05			xxxb
	4	Not used		R/W	0b
	3 - 1	Output De-emphasis RX04			xxxb
	0	Not used			0b
72	7 - 5	Output De-emphasis RX03			xxxb
	4	Not used		R/W	0b
	3 - 1	Output De-emphasis RX02			xxxb
	0	Not used			0b
73	7 - 5	Output De-emphasis RX01			xxxb
	4	Not used		R/W	0b
	3 - 1	Output De-emphasis RX00			xxxb
	0	Not used			0b
74 - 94	All	Reserved	Reserved - Per-Channel Control	R/W	xxh
95	7 - 4	Reserved	Mask Rx LOS Alarm: Writing 1 prevents Int_L on Loss of Signal, Default = 0; mask is required if corresponding optional alarm is implemented.	R/W	0000b
	3 - 0	Mask LOS Flag Rx11 - Rx08			xxxxb
96	all	Mask LOS Flag Rx07 - Rx00		R/W	xxh
97	7 - 4	Reserved	Mask Rx Fault Flag: Writing 1 prevents Int_L on Rx Fault. Default = 0; mask is required if corresponding optional alarm is implemented.	R/W	0000b
	3 - 0	Mask Rx Fault Flag Rx11 - Rx08			xxxxb
98	all	Mask Rx Fault Flag Rx07 - Rx00		R/W	xxh
99	All	Reserved	Reserved - Per Channel Mask	R/W	xxh
100	All	Reserved		R/W	xxh
101	All	Reserved		R/W	xxh
102	All	Mask Pwr Hi-Lo Alarm Rx11 - Rx08	not supported	R/W	xxh
103	All	Mask Pwr Hi-Lo Alarm Rx07 - Rx04		R/W	xxh
104	All	Mask Pwr Hi-Lo Alarm Rx03 - Rx00		R/W	xxh
105	7	Mask Temp High Alarm - Rx	not supported	R/W	xb
	6	Mask Temp Low Alarm - Rx	not supported	R/W	xb
	5 - 0	Reserved		R/W	xxxxxxb
106	7	Mask Vcc3.3 - Rx High Alarm	Mask High Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on High Vcc3.3-Rx Voltage alarm. Default = 0	R/W	xb
	6	Mask Vcc3.3- Rx Low Alarm	Mask High Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on Low Vcc3.3-Rx Voltage alarm. Default = 0	R/W	xb
	5 - 4	Reserved		R/W	xxb
	3	Mask Vcc12-Tx High Alarm	not supported	R/W	xb
	2	Mask Vcc12-Tx Low Alarm	not supported	R/W	xb
	1 - 0	Reserved		R/W	xxb
107	All	Reserved	Vendor Specific Mask	R/W	xxh
108	7 - 4	Reserved		R/W	0000b
	3 - 0	Mask LOL Flag Rx11 - Rx08	Mask Rx LOL Flag: Writing 1 prevents Int_L on Rx Loss of Lock on the Rx CDR. Default = 0, mask is required if corresponding optional alarm is implemented.		xxxxb
109	All	Mask LOL Flag Rx07 - Rx00		R/W	xxh

Dec	Bit	MSA name	MSA description	R/W	Default Value
110 - 115	All	Vendor Specific	Vendor Specific Read - Write Registers for Rx	R	00b
116	7 - 4	Reserved	Rx Output Disable: Writing 1 disables just the output for the channel. Default is 0 (Squelch enabled).	R/W	xxxxb
	3 - 0	Output DisableRx11 -Rx08	1: CDR will be individual bypassed		xxxxb
117	7 - 0	Output Disable Rx07 - Rx00		R/W	xxh
118	All	Reserved		R/W	00b
119	All	Password Change Entry Area	Password Change Entry Area for Rx register space	R/W	xxh
120	All			R/W	xxh
121	All			R/W	xxh
122	All			R/W	xxh
123	All	Password Entry Area	Password Entry Area for Rx register space	W	xxh
124	All			W	xxh
125	All			W	xxh
126	All			W	xxh
127	All	Page Select	Selects Upper Page - Required if paging is used on upper page(s). Not required if paging is not used. Writing 00h selects Tx & Rx Upper Page 00h Writing 01h selects Tx Upper Page 01h, etc.	R/W	xxh

Upper TX Page 01

Dec	Bit	MSA name	MSA description	R/W	Default Value
128	All	Hi Alarm Threshold for 1st Tx Temperature Monitor MSB	Hi Alarm Threshold for 1st Internal Temperature Monitor for Tx MSB: Integer part coded in signed 2's complement. Tolerance is ± 3°C. Set to: 75°C	R	4Bh
129		Hi Alarm Threshold for 1st Tx Temperature Monitor LSB	Hi Alarm Threshold for 1st Internal Temperature Monitor for Tx LSB: Fractional part in units of 1°/256 coded in binary.	R	00h
130	All	Lo Alarm Threshold 1st Tx MonitorTemp	Lo Alarm Threshold for 1st Internal Temperature Monitor for Tx. Same 2 Byte format as 128-129. Set to: -5 °C	R	FBh
131					00h
132	All	Hi Alarm Threshold 2nd Tx MonitorTemp	not supported	R	00h
133					00h
134	All	Lo Alarm Threshold 2nd Tx MonitorTemp	not supported	R	00h
135					00h
136-143	All	Reserved - 8B	Reserved - Alarm Thresholds for Module Monitors	R	00h
144	All	Hi Alarm Treshold Tx Vcc3.3 Monitor	Hi Alarm Threshold for Internal Vcc3.3 Monitor for Tx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Set to: 3,531V	R	89h
145	All			R	EEh
146	All	Lo Alarm Treshold Tx Vcc3.3 Monitor	Lo Alarm Threshold for Internal Vcc3.3 Monitor for Tx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Set to 3,069V	R	77h
147	All			R	E2h
148	All	Hi Alarm Treshold Tx VccHI-Monitor,	Alarm Threshold for Internal VccHU Monitor for Tx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Set to: 4V	R	9Ch
149	All			R	40h
150	All	Lo Alarm Treshold Tx VccHI Monitor	Alarm Threshold for Internal VccHU Monitor for Tx: Voltage in 100 µV units coded as 16 bit unsigned integer, Low byte is MSB. Set to: 0V	R	00h
151	All			R	00h
152 - 167	All	Reserved - 16B	Reserved - Alarm Thresholds for Module Monitors	R	00h
168	All	Hi Alarm Threshold, Tx Bias Current	not supported	R	00h
169	All			R	
170	All	Lo Alarm Threshold, Tx Bias Current	not supported	R	00h
171	All			R	
172	All	Hi Alarm Threshold, Tx Optical Power	not supported	R	00h
173	All			R	
174	All	Lo Alarm Threshold, Tx Optical Power	not supported	R	00h
175	All			R	
176-179	All	Reserved - 4B	Reserved - Alarm Thresholds for Channel Monitors	R	00h
180	All	Checksum	Checksum: Low order 16 bits of the sum of all pairs of bytes from 128 through 175 inclusive, as unsigned integers.	R	xxh
181	All			R	
182	All	Bias Current Monitor Tx11... Bias Current Monitor Tx00	not supported	R	00h
183-205	All				00h
206-229	All	Output Optical Power Monitor Tx11... Output Optical Power Monitor Tx00	not supported	R	00h
230-255	All	Vendor Specific - 26B	Vendor Specific Tx Functions	R	00h

U**pper** RX Page **01**

Dec	Bit	MSA name	MSA description	R/W	Default Value
128	All	Hi Alarm Threshold for 1st Rx Temperature Monitor MSB	not supported, see TX Upper Page	R	00h
129	All	Hi Alarm Threshold for 1st Rx Temperature Monitor LSB	not supported, see TX Upper Page	R	00h
130	All	Lo Alarm Threshold 1st Rx Temp Monitor	not supported, see TX Upper Page	R	00h
131					00h
132	All	Hi Alarm Threshold 2nd Rx Temp Monitor	not supported	R	00h
133					00h
134	All	Lo Alarm Threshold 2nd Rx MonitorTemp	not supported	R	00h
135					00h
136 -143	All	Reserved - 8B	Reserved - Alarm Thresholds for Module Monitors	R	00h
144	All	Hi Alarm Threshold Rx Vcc3.3 Monitor	Hi Alarm Threshold for Internal Vcc3.3 Monitor for Rx: Voltage in 100 uV/units coded as 16 bit unsigned integer, Low byte is MSB. Set to: 3,531V	R	89h
145	All			R	EEh
146	All	Lo Alarm Threshold Rx Vcc3.3 Monitor	Lo Alarm Threshold for Internal Vcc3.3 Monitor for Rx: Voltage in 100 uV/units coded as 16 bit unsigned integer, Low byte is MSB. Set to 3,069V	R	77h
147	All			R	E2h
148	All	Hi Alarm Threshold Rx Vcc12-Monitor	not supported	R	00h
149	All			R	00h
150	All	Lo Alarm Threshold Rx Vcc12 Monitor	not supported	R	00h
151	All			R	00h
152-167	All	Reserved - 16B	Reserved - Alarm Thresholds for Module Monitors	R	00h
168 -175	All	Reserved - 4B	Reserved Alarm Thresholds for Channel Monitors	R	00h
176	All	Hi Alarm Threshold, Rx Optical Power	not supported	R	00h
177	All			R	
178	All	Lo Alarm Threshold, Rx Optical Power	not supported	R	00h
179	All			R	
180	All	Checksum	Checksum: Low order 16 bits of the sum of all pairs of bytes from 128 through 175 inclusive, as unsigned integers.	R	xxh
181	All			R	
182 - 205	All	Reserved - 48B	Reserved Rx Channel Monitors	R	00h
206 - 229	All	Input Optical Power Monitor Rx11... Input Optical Power Monitor Rx00	not supported	R	00h
230 - 255	All	Vendor Specific - 26B	Vendor Specific Rx Functions	R	00h

Upper TX RX Page 00

Dec	Bit	MSA name	MSA description	ASCII	R/W	Default Value
128	7	Reserved - Type Identifier	OBT (not defined in MSA)		R	00h
129	7 .. 5	Power Class	000: 0.25W max - Class 0 001: 1.0W max - Class 1 010: 1.5W max - Class 2 011: 2.5W max - Class 3 100: 4.0W max - Class 4 101: 6.0W max - Class 5 **110: >6.0W - Class 6** 111: Reserved		R	110b
	4	Tx CDR Presence	Coded 1 for Tx CDR (clock & data recovery) provided; else coded 0		R	1b
	3	Rx CDR Presence	Coded 1 for Rx CDR provided; else coded 0		R	1b
	2 .. 0	Reserved			R	000b
130	All	Connector / Cable	00h-0Ch: Not compatible w/CXP, Rsvd.-compatibility 0Dh-1Fh: Reserved 20h-23h: Rsvd.-compatibility 24h-2Fh: Reserved 30h: Passive Copper Cable Assembly 31h: Active Copper Cable Assembly (ref. Byte 147) 32h: Active Optical Cable Assembly **33h: Optical Transceiver w/ optical connector** 34h-7Fh: Reserved 80h-FFh: Vendor Specific		R	33h
131	7	1	3.3V - Vcc3.3 - Coded 1 if required for the module		R	1b
	6 .. 4	000b - Reserved	2.5V, 1.8V, Vo supplies - not available in receptacle		R	000b
	3	1	12V - Vcc12 - Coded 1 if required for the module		R	0b
	2 .. 0	000b - Reserved	Note: Module requires VddHI > 3.3V -- but not defined in MSA, therefore information not coded in register 131		R	000b
132	All	Max Temperature	Max Recommended Operating Case Temperature for the module, in Degrees C		R	46h
133	All	Min per-channel bit rate	Min signal rate = binary value x 100 Mb/s (e.g., 25 (00011001b) = 2500 Mb/s, & 100 (01100100b) = 10,000 Mb/s)		R	0Ch
134	All	Max per-channel bit rate	Max signal rate = binary value x 100 Mb/s		R	FFh
135	All	Laser Wavelength	Nominal Laser Wavelength (Wavelength in nm = value / 20): e.g.: 4268h = 17000, 17000/20 = 850 nm		R	42h
136						68h
137	All	Max Wavelength Deviation	Optical: Wavelength deviation from nominal (Wavelength tolerance in nm = +/- value / 200): e.g.: 7D0h = 2000, 2000/200= 10 nm		R	07h
138	All					D0h
139	7	Support for Tx Fault	Coded 1 if Tx Fault Flag supported, else coded 0		R	1b
	6	Support for Rx Fault	Coded 1 if Rx Fault Flag supported, else coded 0		R	1b
	5	Support for Tx LOS	Coded 1 if Tx Loss of Signal Flag supported, else coded 0		R	1b
	4	Support for Rx LOS	Coded 1 if Rx Loss of Signal Flag supported, else coded 0		R	1b
	3	Support for Tx Squelch	Coded 1 if Tx Squelch supported, else 0		R	1b

Dec	Bit	MSA name	MSA description	ASCII	R/W	Default Value
	2	Support for Rx Squelch	Coded 1 if Rx Squelch supported, else 0		R	1b
	1	Support for Tx CDR LOS	Coded 1 if Tx CDR Loss of Sync Flag supported, else coded 0		R	1b
	0	Support for Rx CDR LOS	Coded 1 if Rx CDR Loss of Sync Flag supported, else coded 0		R	1b
140	7	Support for Tx Bias Monitor	Coded 1 if Tx Bias Monitor supported, else coded 0		R	0b
	6	Support for Tx LOP Monitor	Coded 1 if Tx Light Output Power Monitor supported, else coded 0		R	0b
	5	Support for Rx Input Power Monitor	Coded 1 if individual Rx Input Power Monitors supported, coded 0 for single-channel or group monitor		R	0b
	4	Support for Rx Input Power Format	Coded 1 if Rx Input Power reported as Pave, coded 0 for reported as OMA		R	0b
	3	Support for Case Temp Monitor	Coded 1 if Case Temperature Monitor supported, else coded 0		R	0b
	2	Support for Rx Input Power Format	Coded 1 if Internal Temperature Monitor supported, else coded 0		R	1b
	1	Support for Peak Temp Monitor	Coded 1 if Peak Temperature Monitor supported, else coded 0		R	0b
	0	Support for Elapsed Time Monitor	Coded 1 if Elapsed PowerOn Operating Time Monitor supported, else coded 0		R	0b
141	7	BER Monitor	Coded 1 for BER Monitor, else coded 0		R	0b
	6	Vcc3.3-Tx Monitor	Coded 1 for Internal Vcc3.3-Tx Monitor, else coded 0		R	1b
	5	Vcc3.3-Rx Monitor	Coded 1 for Internal Vcc3.3-Rx Monitor, else coded 0		R	1b
	4	VccHI-Tx Monitor	Coded 1 for Internal VccHI-Tx Monitor, else coded 0		R	1b
	3	VccHI-Rx Monitor	Coded 1 for Internal Vcc12-Rx Monitor, else coded 0		R	0b
	2	TEC Current Monitor	Coded 1 for TEC current Monitor, else coded 0		R	0b
	1 .. 0	Reserved			R	00b
142	7 .. 6	Tx Channel Disable Capabilities	00: Not provided, or unspecified 01: Global Tx Channel Disable Control implemented 10: Individual & independent Tx Channel Disable Control implemented 11: Reserved		R	10b
	5 .. 4	Tx Channel Output Disable Capabilities	00: Not provided, or unspecified 01: Tx Global Channel Output Disable Control implemented 10: Individual & independent Tx Channel Output Disable Control implemented 11: Reserved		R	10b
	3 .. 2	Tx Squelch Disable Capabilities	00: Not provided, or unspecified 01: Global Tx Squelch Disable Control implemented 10: Individual and independent Tx Channel Squelch Control implemented 11: Reserved		R	10b
	1	Tx Polarity Flip Mode	Coded 1 for Tx Channel Polarity Flip Control provided, else coded 0		R	1b
	0	Tx Margin Mode	Coded 1 for Tx Margin Mode provided, else coded 0		R	0b
143	7 .. 4	Reserved			R	0000b

Dec	Bit	MSA name	MSA description	ASCII	R/W	Default Value
	3 .. 2	Tx Input Equalization Control	00: Not provided, or unspecified 01: Global Tx Input Equalization Control implemented 10: Individual and independent Tx Input Equalization Control implemented 11: Reserved		R	10b
	1 … 0	Tx Rate Select Control	00: Not provided, or unspecified 01: Global Tx Rate/Application Select Control implemented 10: Reserved (Individual and independent Tx Rate/Application Select control not available except in vendor-specific manner). 11: Reserved		R	00b
144	7 .. 6	Rx Channel Disable Capabilities	00: Not provided, or unspecified 01: Global Rx Channel Disable Control implemented 10: Individual & independent Rx Channel Disable Control implemented 11: Reserved		R	10b
	5 .. 4	Rx Channel Output Disable Capabilities	00: Not provided, or unspecified 01: Rx Global Channel Output Disable Control implemented 10: Individual & independent Rx Channel Output Disable Control implemented 11: Reserved		R	10b
	3 .. 2	Rx Squelch Disable Capabilities	00: Not provided, or unspecified 01: Global Rx Squelch Disable Control implemented 10: Individual and independent Rx Channel Disable Control implemented 11: Reserved		R	10b
	1	Rx Polarity Flip Mode	Coded 1 for Rx Channel Polarity Flip Control provided, else coded 0		R	1b
	0	Rx Margin mode	Coded 1 for Rx Margin Mode provided, else coded 0		R	0b
145	7 .. 6	Reserved				
	5 .. 4	Rx Output Amplitude Control	00: Not provided, or unspecified 01: Global Rx Output Amplitude Control implemented 10: Individual and independent Rx Output Amplitude Control implemented 11: Reserved		R	10b
	3 .. 2	Rx Output De-Emphasis Control	00: Not provided, or unspecified 01: Global Rx Output De-Emphasis Control implemented 10: Individual and independent Rx Output De-Emphasis Control implemented 11: Reserved		R	10b
	1 .. 0	Rx Rate Select Control	00: Not provided, or unspecified 01: Global Rx Rate/Application Select Control implemented 10: Reserved (Individual and independent Rx Rate/Application Select control not available except in vendor-specific manner). 11: Reserved		R	00b
146	7	FEC Control	Coded 1 for FEC Control, else coded 0		R	0b

Dec	Bit	MSA name	MSA description	ASCII	R/W	Default Value
	6	PEC Control	Coded 1 for PEC Control, else coded 0		R	0b
	5	JTAG Control	Coded 1 for JTAG Control, else coded0		R	0b
	4	AC-Jtag Control	Coded 1 for AC-JTAG Control, else coded 0		R	0b
	3	BIST	Coded 1 for BIST, else coded 0		R	0b
	2	TEC Temperature Control	Coded 1 for TEC Temperature Control, else coded 0		R	0b
	1	Sleep Mode Set Control	Coded 1 for Sleep Mode Set Control provided, else coded 0		R	0b
	0	CDR Bypass Control	Coded 1 for CDR Bypass Control provided, else coded 0		R	1b
147	7 .. 4	Device Technology	0000: 850 nm VCSEL 0001:1310 nm VCSEL 0010:1550 nm VCSEL 0011: 1310 nm FP 0100:1310 nm DFB 0101:1550 nm DFB 0110: 1310 nm EML 0111: 1550 nm EML 1000: Copper or others 11001: 1490 nm DFB 1010: Copper cable un-equalized 1011: Copper cable passive equalized 1100: Copper cable near & far end active equalizers 1101: Copper cable, far end active equalizer 1110: copper cable, near end active equalizer 1111: Reserved		R	0000b
	3	Wavelength Control	0: No control 1: Active wavelength control		R	0b
	2	Transmitter cooling	0: Uncooled transmitter, 1: Cooled transmitter		R	0b
	1	Optical Detector	0: P-I-N Detector 1: APD detector		R	0b
	0	Optical Tunability	0: Transmitter not tunable, 1:Transmitter tunable		R	0b
148	All	Max Power Utilization	Maximum power utilization, in units of 0.1 Watts. Range: 0.1W - 25.5 Watts 00h: No information Set to 7,9W		R	4Fh
149	7 .. 1	Data rates supported	Bit 7 = IEEE 802.3 CPPI supported Bit 6 = Reserved Bit 5 = EDR supported Bit 4 = FDR supported, CDR bypassed Bit 3 = QDR supported, CDR bypassed Bit 2 = DDR supported, CDR bypassed Bit 1 = SDR supported, CDR bypassed		R	0011111b
	0	12x to 3-4x	Coded 1 for 12x to 3-4x Cable, else, for regular cable without fanout, coded 0		R	0b
150	All	Cable Length	Physical length of cable, in units of 0.5 meters Range: 0.5 - 32767 m 0000h: Optical transceiver with mateable optical connector		R	00h
151	All				R	00h
152	All	Vendor Name	Vendor name in ASCII - 16B	F	R	46h
153	All			C		43h
154	All			I		49h
155	All					20h
156	All			M		4Dh
157	All			e		65h
158	All			r		72h

Dec	Bit	MSA name	MSA description	ASCII	R/W	Default Value
159	All			g		67h
160	All			e		65h
161	All			O		4Fh
162	All			p		70h
163	All			t		74h
164	All			i		69h
165	All			c		63h
166	All			s		73h
167	All					20h
168	All	Vendor OUI	Vendor OUI (IEEE ID): Organization-Unique Identifier - 3B		R	**00h**
169	All					**0Ah**
170	All					**0Dh**
171-186	All	Vendor Part Number	Vendor Part Number in ASCII - 16B		R	
187	All	Vendor Rev. Number	Vendor Revision Number in ASCII - 2B		R	
188	All					
189-204	All	Vendor Serial Number	Vendor Serial Number (ASCII): Varies by unit - 16B		R	
205	All	Vendor Date Code	Vendor Date Code YYYYMMDD (ASCII): Spaces (20h) for unused characters	y	R	
206	All			y		
207	All			y		
208	All			y		
209	All			m		
210	All			m		
211	All			d		
212	All			d		
213	All	Lot Code	Customer-Specific Code or Vendor-Specific lot code (ASCII). 10B. All spaces (20h) if unused		R	
214	All					
215	All					
216	All					
217	All					
218	All					
219	All					
220	All					
221	All					
222	All					
223	All	Checksum	Checksum of addresses 128 through 222 inclusive: 8 low-order bits of sum		R	
224-255	All	Vendor Specific - 32B	Vendor Specific Read-Only Registers		R	

Upper Page 2

Dec	Bit	MSA name	MSA description	R/W	Default Value
128-255	All	Reserved	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI Notes: code for the module.	R/W	00h

NOTE: Area is by default Password Protected
Access is possible via TX Password Entry Area or RX Password Entry Area at Lower Pages, Register 7Bh to 7Eh.
Inital password is 00h 00h 10h 11h.

Non-Volataile Registers

Mechanical Specification

The OBT is illustrated in Figure 9 without heat sink as an example.

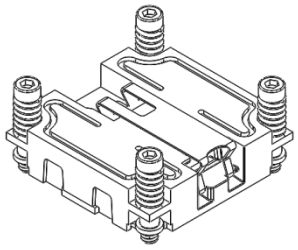


Figure 9 Illustration of the OBT base module and MT ferrule clip

Torque of the Screws is defined with 0.072 +/-0.017 Nm.

For OBT base module different heat sink designs available for the OBT base module.
For further details please note the customers drawings with Base Reference Number 10124588 for 12 Channel version. Use Base Reference Number 10135828 for the 8 Channel version.
Both documents are available on request.

OBT Optical Port Pin Layout

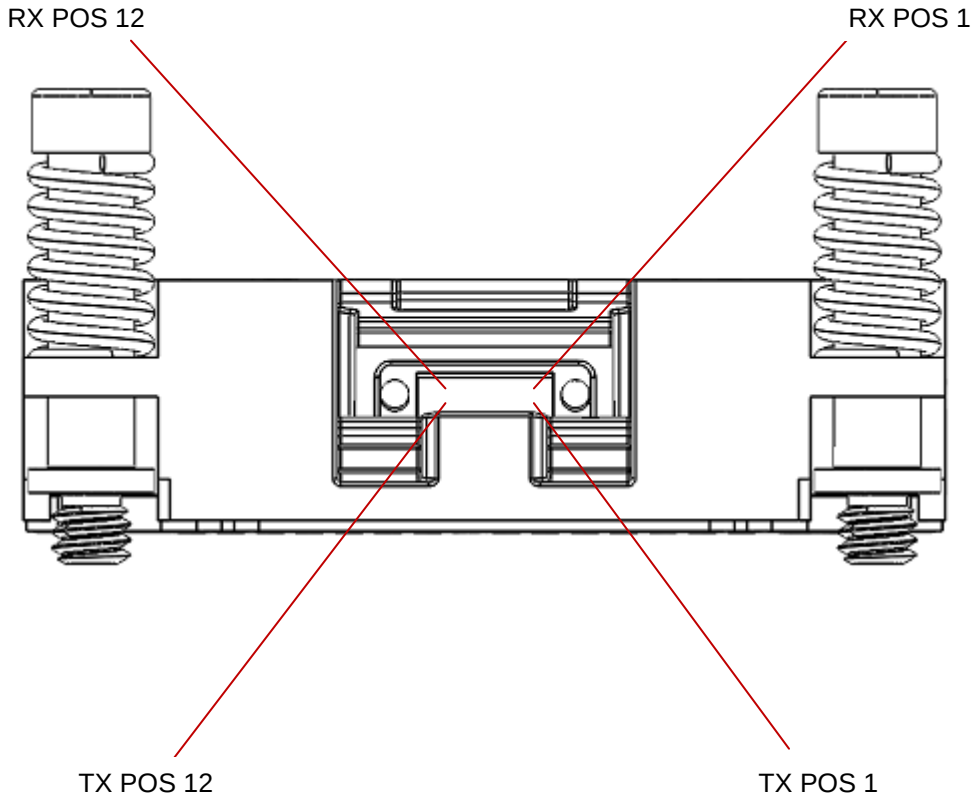
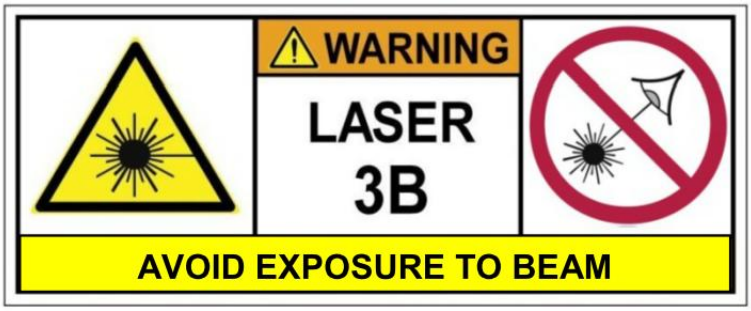


Figure 10 Optical Port Pin Layout

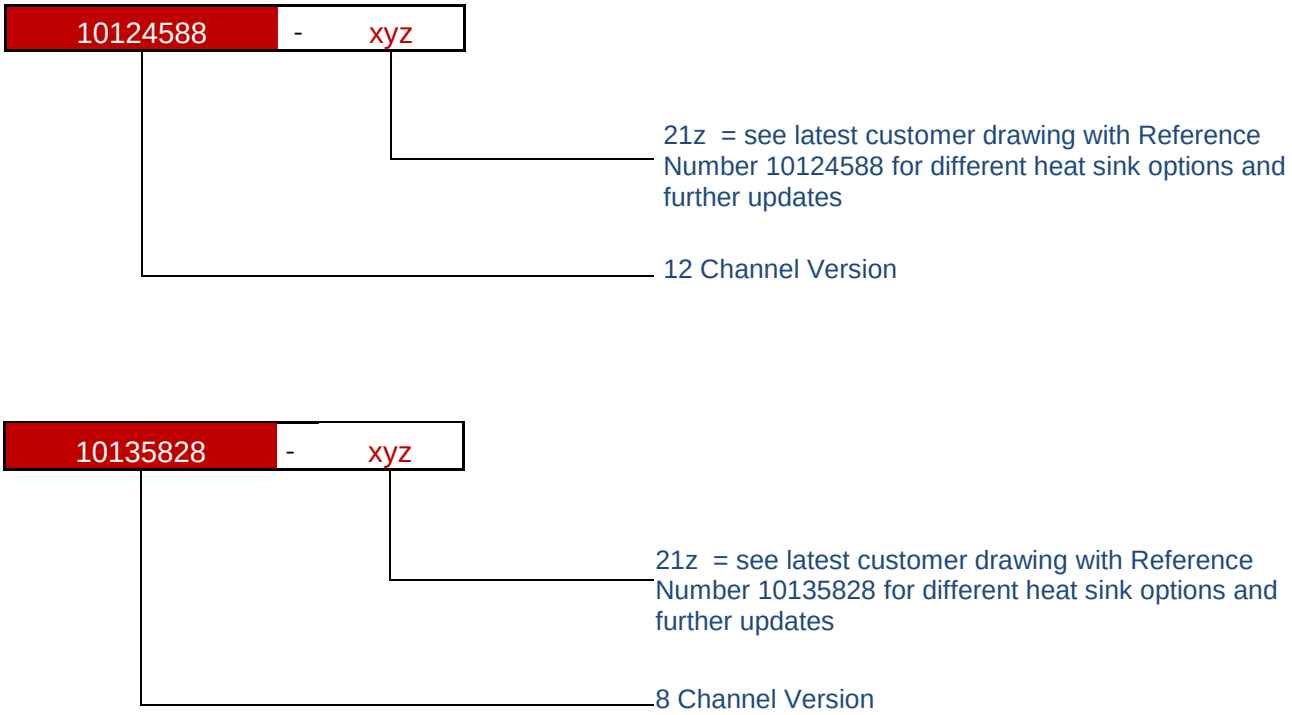
Eye Safety

CLASS 3B
LASER PRODUCT



This laser based multimode Onboard Transceiver is a Class 3b product. It complies with IEC 60825-1 (2007/Edition 2, 2014/Edition 3) and FDA performance standards for laser products (21 CFR 1040.10 and 1040.11) except for deviations pursuant to Laser Notice 50, dated June 24, 2007.

Product Number Scheme



Revision Handling

Revision	Description	Date	Author
1.0	Initial Version	11/11/2015	KSCH
1.1	General change over to support of BER better then 1E-12 • Implement Nomenclature at page 4 • Implement statement for VddHI, Power Sequencing at page 8 • Extend Figure 3 Tx CDR bypass • Extend Figure 4 Rx CDR bypass • Change to BER=1E-12 at Table 4 • Update Power Consumption at Table 5 • Correction Figure 5 • Update Table 6, change to CDR Loop bandwidth information • General Updates at Table 9 and Table 10 for optical parameters • Implement condition notes for EH15 and EW15 parameters, Table 11 • Update Input Voltage High Parameter at Table 12 and Table 13 • Note for Memory Page 2 support at Figure 8 • Update description for chapter Receiver *Voltage Output Swing and Emphasis Setting* • Update Memory Map Table Lower Receiver Memory Page, Register 62 to 73 • Add in Chapter Mechanical Specification a reference number for Customer Drawing at Page 44 • Add information for Torque of OBT Screws at Page 44 • Update of Product Number Scheme Minor text corrections	06/28/2016	KSCH
1.2	• Implement Pin Description Table 1	07/07/2016	KSCH