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DSH Interface Verification System

Introduction

The DSH Interface Verification System (IVS) is a system using a TALON-DX signal processing board to implement a packet receiver (CSP side) which can be used to verify the interface between DSH and CSP.

In order to test the DSH IVS independently of the DSH Element, a packet generator will also be developed to run on the TALON-DX.

The software and firmware developed for the DSH IVS should be re-usable for Mid.CBF where appropriate and will follow SKA standards and processes. Re-usable firmware IP blocks are indicated by Mid.CBF part numbers in Figure 4.

Requirements

1. The DSH IVS shall receive 100 GbE packets using QSFP28 100GBase-SR4 or 100GBase-LR4 fiber optical modules on the TALON-DX signal processing board.
2. The DSH IVS shall verify that content of packets received conform to the DSH-CSP ICD.
3. The DSH IVS shall count and report valid packets received and error conditions encountered:
    a. Ethernet CRC errors (TBD)
    b. Unexpected header field contents
    c. Incorrect sample counts between 1PPS marks
4. The DSH IVS shall capture sufficient consecutive complete packets in on-chip FPGA memory to compute the following statistics on the data content:
    a. State counts / histogram
    b. Mean
    c. Standard deviation
5. The DSH IVS shall have a mode of operation where the data content of packets is checked against an expected pattern and any errors detected are reported.
6. The DSH IVS shall be able to generate packets according to the DSH-CSP ICD and transmit 100 GbE packets using QSFP28 100GBase-SR4 or 100GBase-LR4 fiber optical modules on the TALON-DX signal processing board.
7. The DSH IVS shall be able to generate packet contents of the following forms:
    a. Known pattern which can be checked by the receiver
    b. Gaussian noise with a specified mean and standard deviation

    c. Test vectors with simulated astronomical data suitable for testing signal processing.
8. The DSH IVS shall be able to generate packets with the following error conditions:
    a. Ethernet CRC errors (TBD)
    b. Unexpected header field contents
    c. Incorrect sample counts between 1PPS marks
9. The DVS IVS shall support two forms of test vector generation:
    a. Short sequence test vectors (SSTV) in on-chip FPGA memory
    b. Long sequence test vectors (LSTV) in DDR4 RAM.
10. For both types of test vectors, the DVS IVS shall repeat the test vector but generate packets with header information that indicate continually sequential data packets (packet numbers and timestamps do not repeat).
11. The DSH IVS shall be able to generate, receive and verify packets for SKA Band 1, 2 & 5 as specified in the DSH-CSP ICD.
12. A single TALON-DX board shall be able to operate as a packet receiver, packet generator or both.
13. The DSH IVS packet generators and receivers shall be configurable using a graphical user interface.
14. The DSH IVS packet generators and receivers shall be configurable programmatically in order to facilitate automated testing.

Context

There are three possible contexts the DSH IVS can operate in and diagrams are shown below.

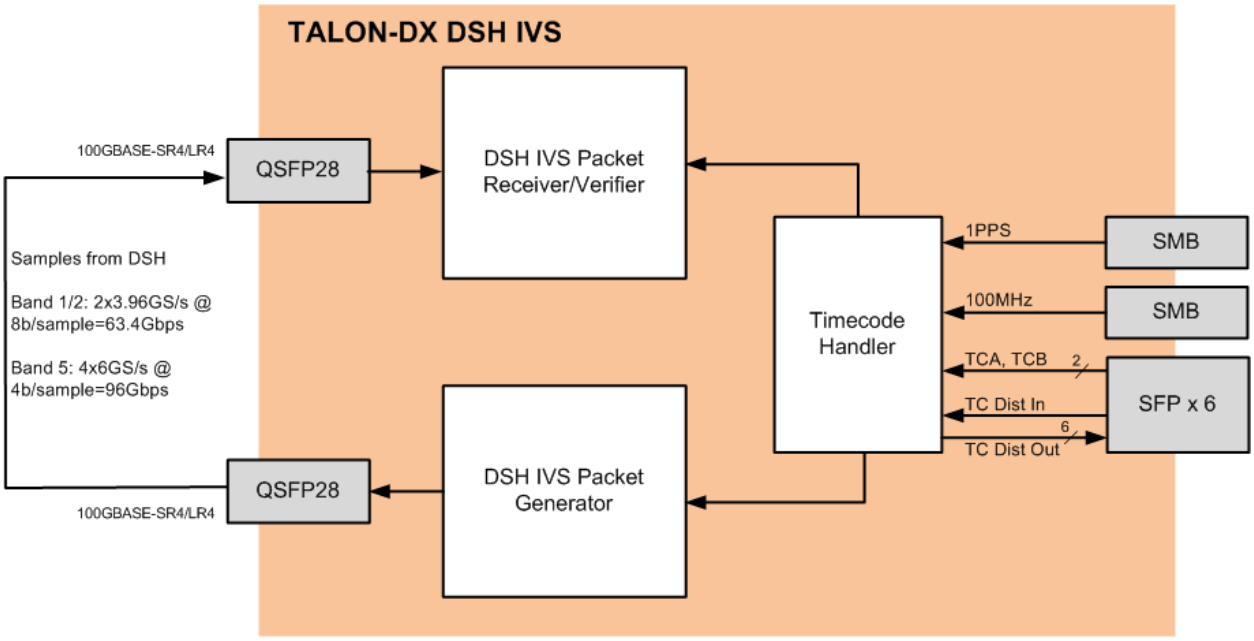

Figure 1 One TALON-DX DSH IVS generating packets on one QSFP28, optically connected to the other QSFP28 which is receiving/verifying packets.

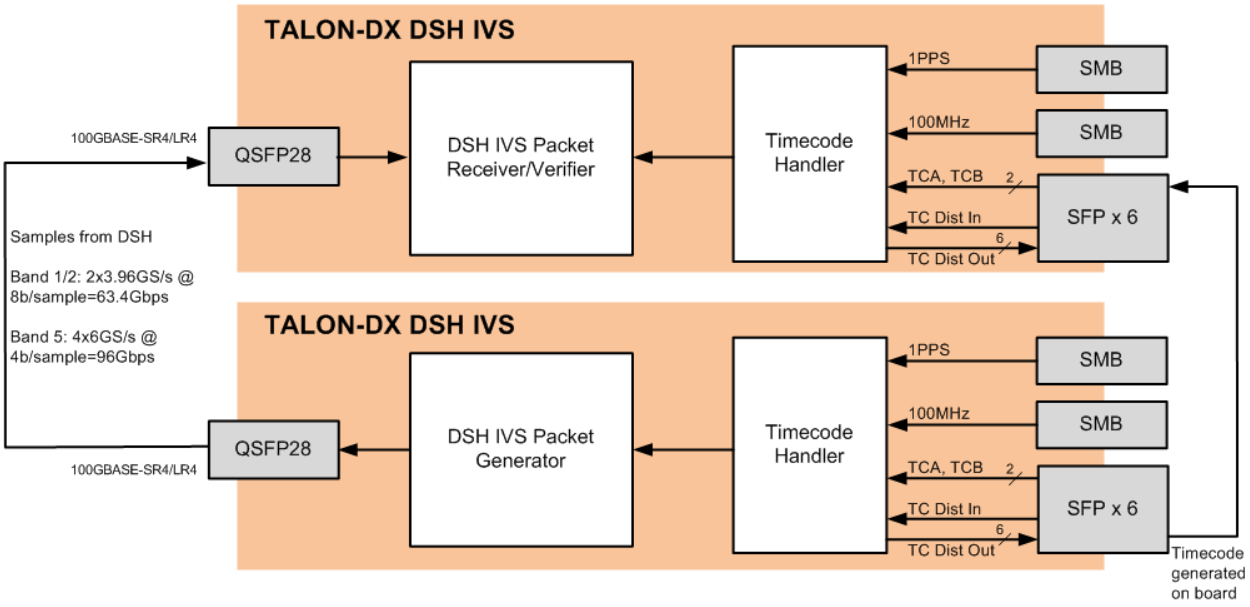

Figure 2 Two TALON-DX DSH IVS, one generating packets and the other receiving/verifying packets.

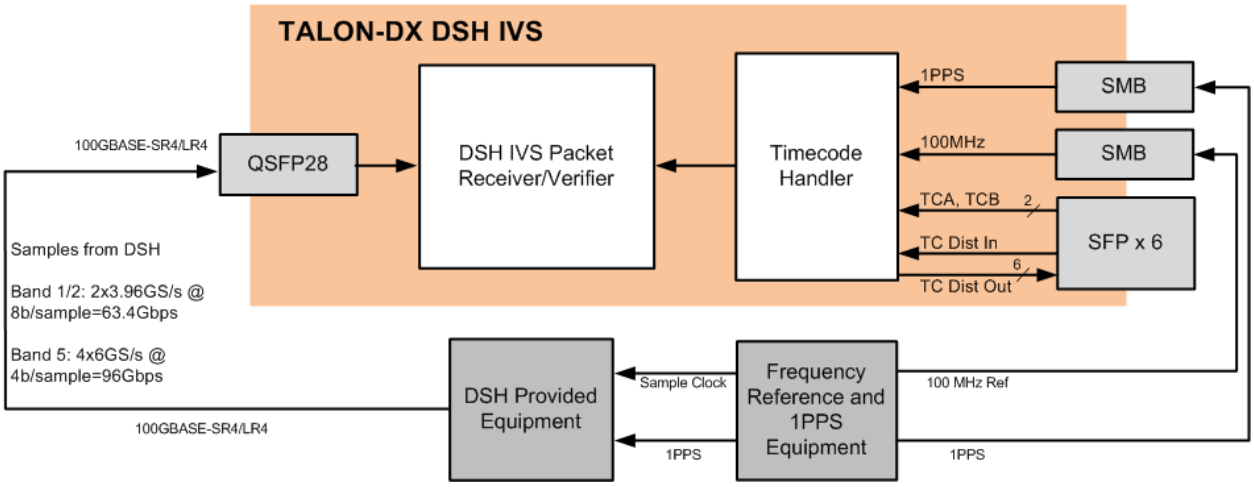

Figure 3 One TALON-DX DSH IVS receiving packets generated by DSH provided equipment.

Firmware

The firmware running on the TALON-DX FPGA is shown in the figure below and brief descriptions on each firmware block follow.

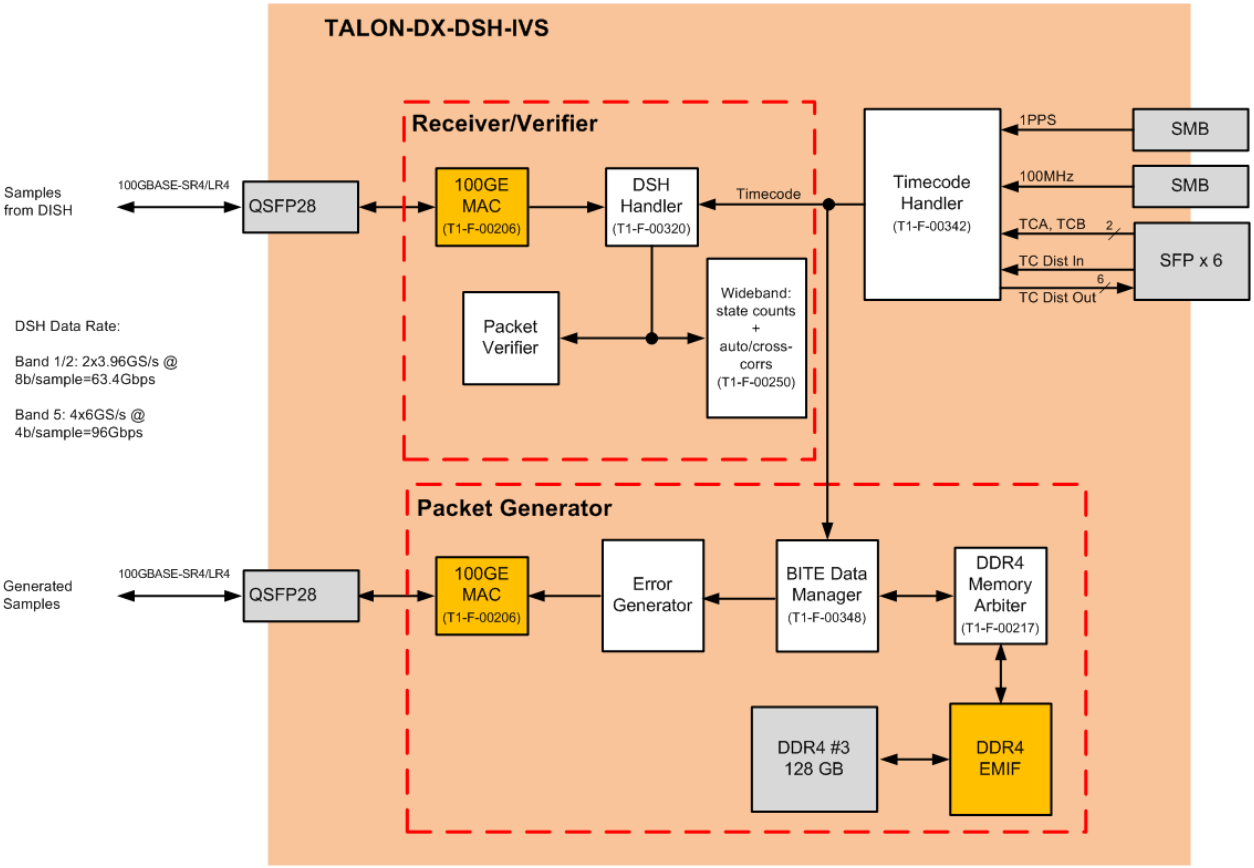

Figure 4 DSH IVS IP blocks running on TALON-DX FPGA

Table 1 IP Block Descriptions

IP Block	Description
100GE MAC	Soft 100 Gigabit Ethernet MAC IP block provided by Intel
DSH Handler	IP to interface with the 100GbE MAC and perform basic verification of DSH packets. This includes monitoring CRC errors detected by the MAC, checking packet sequence numbers, timestamps, number of samples between 1PPS, etc. Reports valid packet count and error counts.
Wideband state counts + auto/cross corr	Captures a number of sequential packets (headers and data) into on-chip memory and notifies HPS when buffer is ready. After HPS indicates that data has been transferred, capture begins again.
Packet Verifier	Verifies contents of the packets is as expected when operating in pattern mode and reports valid packet counts and error counts.
BITE Data Manager	Receives test vectors generated by the HPS and stores them in on-chip or DDR4 memory. Repeatedly reads test vectors from memory and forms DSH packets with correct header information and transmits 100 GbE MAC. Sample rate and bits/per sample can be configured.
Error Generator	Provides the capability to inject errors into the data packets generated by the BITE Data Manager IP block.
DDR4 Memory Arbiter	IP that provides an arbiter so one DDR4 EMIF can be shared by multiple IP blocks. This is not explicitly required for the DSH IVS, but the BITE Data Manager in Mid.CBF will require DDR4 access through an arbiter.
DDR4 EMIF	DDR4 External Memory Interface Hard IP provided by Intel.
Timecode Handler	IP that can generate a timecode signal either from external 100 MHz clock and 1PPS or from internal clocks. The timecode is distributed internally to other IP blocks and output on fiber optic timecode distribution ports.

Software

Software is broken down into components that are running on the HPS and components that are running on a standard Linux server. TANGO will be used for communication between the server and HPS. Each firmware IP block will have a TANGO device running on the HPS and a GUI that can be run on the server for monitor and control. A top level TANGO device (DSH IVS device) running on the server will provide monitor and control of the DSH IVS as a whole. The DSH IVS device can be controlled via a GUI or programmatically for automated testing.

The following two tables provide brief descriptions of software components running on the HPS and server.

Table 2 HPS Software Components

IP Block	Description
100GE MAC Device	TANGO device to monitor and control of the 100 GbE MAC (TBD if required).
DSH Handler Device	TANGO device to monitor and control of the DSH Handler IP block.
Wideband state counts + auto/cross corr Device	TANGO device to monitor and control of the Wideband state count + auto/cross corr IP block. This includes retrieving buffered data from FPGA DDR4, calculating statistics on the data and performing auto/cross correlation of the data.
Packet Verifier Device	TANGO device to monitor and control of the Packet Verifier IP block.
BITE Data Manager Device	TANGO device to monitor and control BITE Data Manager IP block. This includes facilities to transfer test vectors into on-chip FPGA memory or DDR4 via the BITE Data Manager and start packet transmission, monitor packets sent, etc.
Error Generator Device	TANGO device to monitor and control the Error Generation IP block.
DDR4 Memory Arbiter Device	TANGO device to monitor and control DDR4 Memory Arbiter IP (TBD if required).
DDR4 EMIF Device	TANGO device to monitor and control DDR4 EMIF hard IP (TBD if required).
Timecode Handler Device	TANGO device to monitor and control Timecode Handler IP. This included controlling the operating mode (external 100 MHz/1PPS vs internal) and enabling timecode outputs.
Pattern Generator Device	TANGO device to generate test vectors that follow a known pattern and pass it to BITE Data Manager device.
Gaussian Noise Generator Device	TANGO device to generate Gaussian noise with configurable mean and standard deviation and pass it to BITE Data Manager device.
Astronomical Test Vector Generator Device	Software to generate test vectors that contain astronomical signals and noise which are suitable for testing signal processing algorithms and pass it to BITE Data Manager device.

Table 3 Server Software Components

IP Block	Description
100GE MAC GUI	GUI to monitor and control of the 100 GbE MAC (TBD if required).
DSH Handler GUI	GUI to monitor and control of the DSH Handler IP block.
Wideband state counts + auto/cross corr GUI	GUI to monitor and control of the Wideband state count + auto/cross corr IP block. This includes plotting histograms and auto/cross correlation results, displaying packet details, etc.
Packet Verifier GUI	GUI to monitor and control of the Packet Verifier IP block.
Error Generator GUI	GUI to monitor and control of the Error Generator IP block.
DDR4 Memory Arbiter GUI	GUI to monitor and control DDR4 Memory Arbiter IP (TBD if required).
DDR4 EMIF GUI	GUI to monitor and control DDR4 EMIF hard IP (TBD if required).
Timecode Handler GUI	GUI to monitor and control Timecode Handler Ip block.
Packet Generator Device	TANGO device to allow monitor and control of the packet generation functions of the DSH IVS. This include high level functions for selecting type test vector, duration of test vector, errors to introduce, etc.
Packet Generator GUI	GUI to monitor and control packet generation functions.
Packet Receiver Device	TANGO device to allow monitor and control of the packet receiver/verifier functions of the DSH IVS. This includes configuring the mode of operation and reporting results.
Packet Receiver GUI	GUI to monitor and control the packet receiver/verifier functions.

Development Plan

The development of the DSH IVS will be done using a SAFe development team. The priority of functionality is as follows:

1. 100GbE communication using 100GBase-SR4 QSFP28 modules.
2. Generation and transmission of DSH packets with a known pattern using on-chip memory.
3. Reception and verification of DSH packets with a known pattern.
4. Inject errors in packet generation.
5. Internal timecode generation and two board synchronization.
6. 100GbE communication using 100GBase-LR4 QSFP28 modules.
7. Generation and transmission of DSH packets with a known pattern using DDR4 memory.
8. Time generation from external 100 MHz and 1PPS.
9. Generate DSH packets containing Gaussian noise (on-chip and DDR4 memory).
10. Calculate statistics and auto/cross correlations on Gaussian noise packets.
11. Generate DSH packets with simulated astronomical signals (on-chip and DDR4 memory).
12. Test with DSH provided equipment (TBD).

Equipment

1. TALON-DX board with complete board support package.
2. 100GBase-SR4 QSFP28 optical modules
3. MTP-to-MTP 12 fiber OM4 multi-mode fiber optical cable
4. 100GBase-LR4 QSFP28 optical modules

5. LC-to-LC 2 fiber single mode fiber optical cable
6. Linux Server
7. Sample clock, 100 MHz reference and 1PPS generation equipment
8. DSH Element provided packet generation equipment